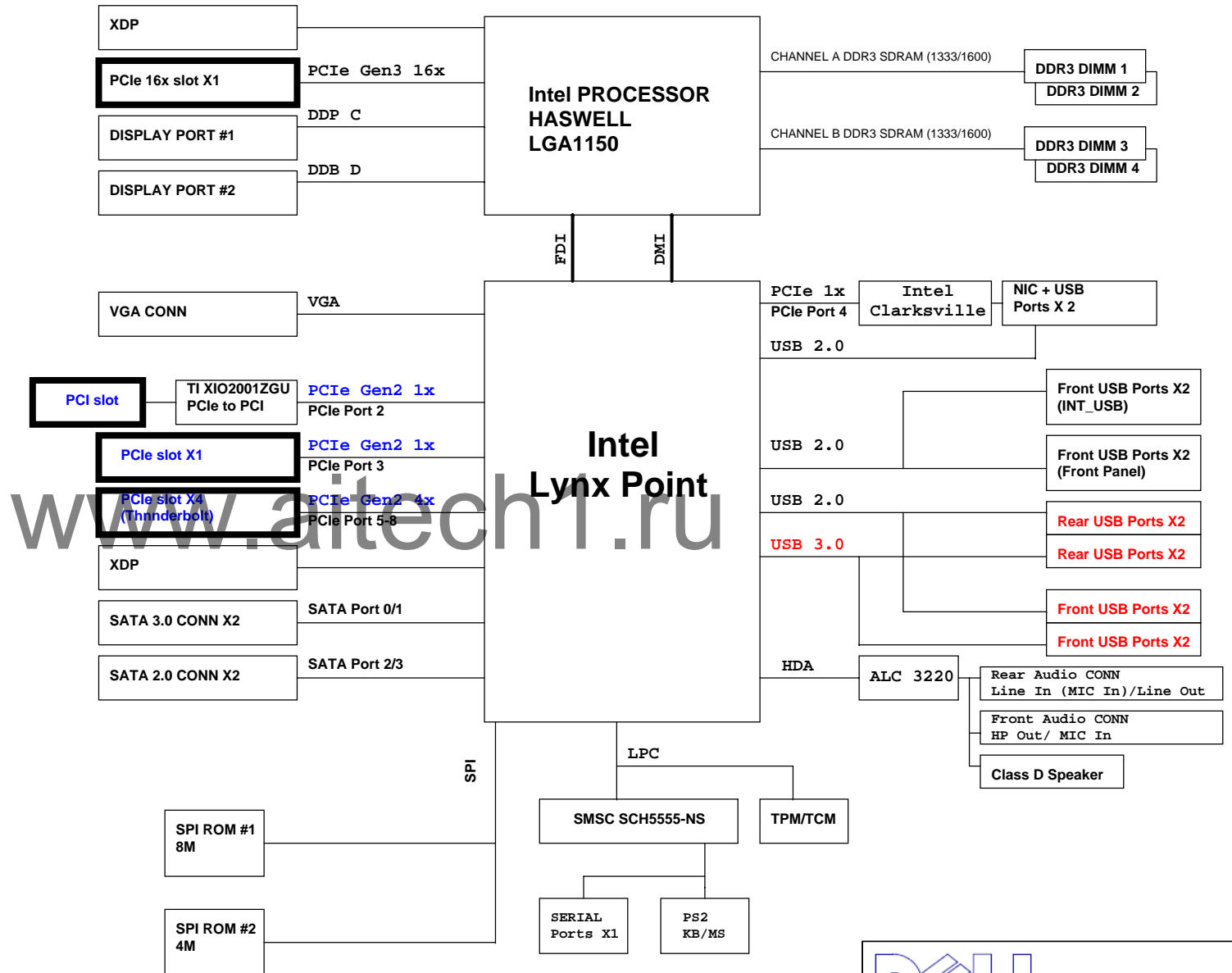
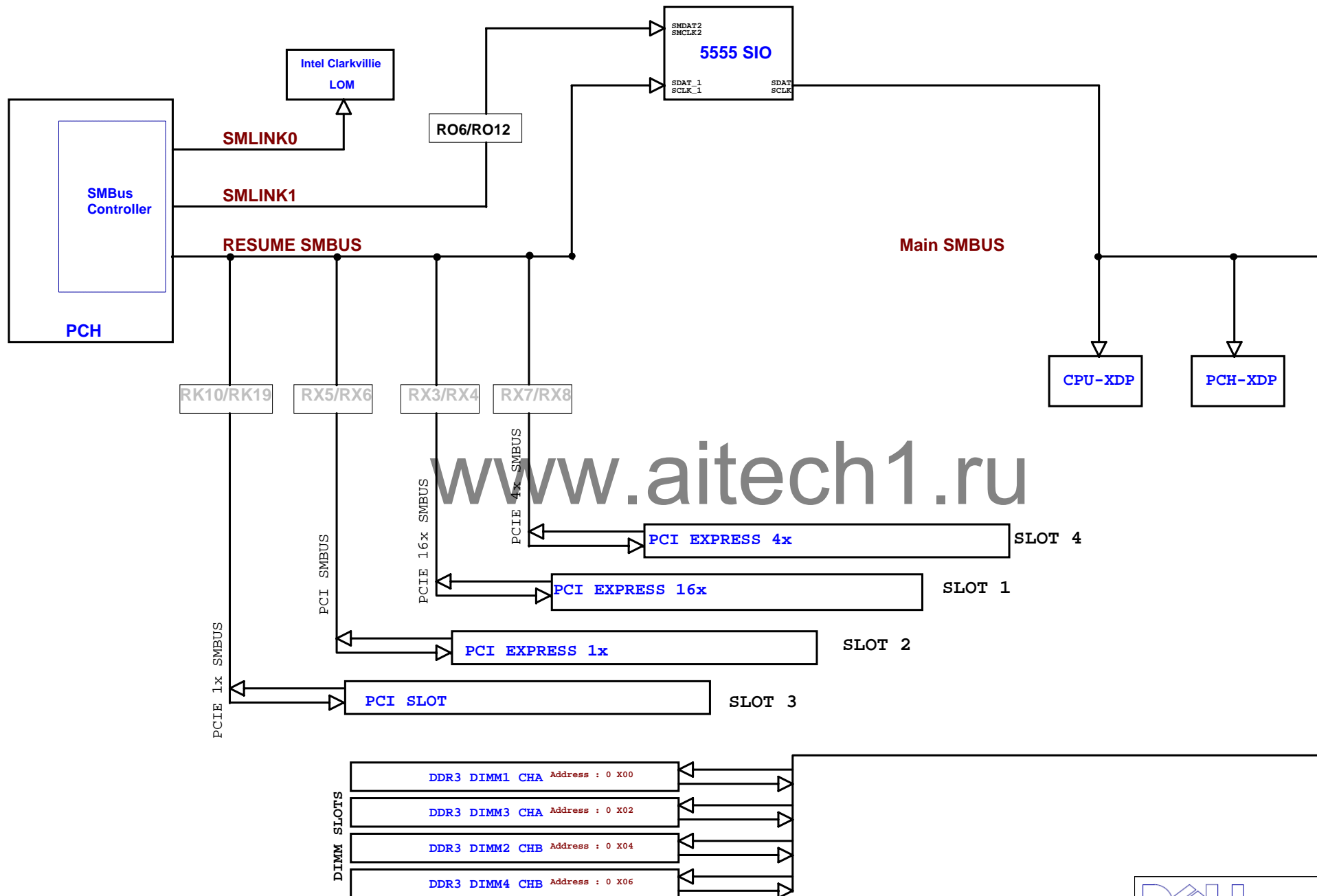


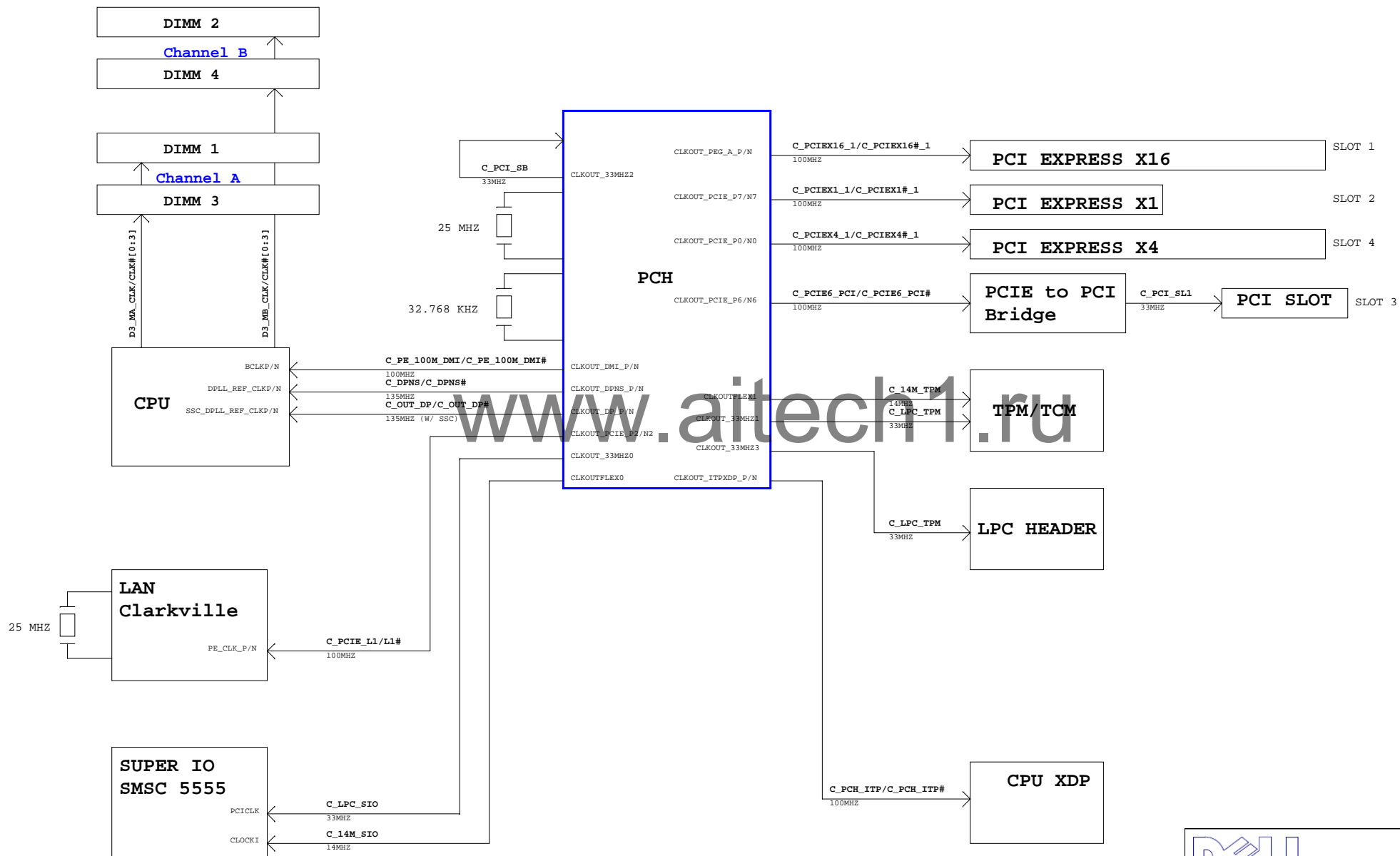
Tulum/Amazon MT

1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. Strap/IRQ/IDSel Table
8. GPIO Table
- 9-14. CPU
- 15-16. DDR3 Conn: CHA
- 17-18. DDR3 Conn: CHB
19. Label
20. TBT_HDR
- 21-28. PCH
- 29-30. SIO SCH5555-NS
- 31-32. LAN
- 33-34. Audio
35. Slot4 : PCIe 4X
36. Slot1 : PCIe 16X
37. Slot3 : PCI
38. Slot2 : PCIe 1X
- 39-40. Display Port
41. VGA
42. SATA
43. Rear USB
44. TPM & TCM
45. FAN
46. Thermal Sensor Conn
47. PS2
48. COM1
49. SPI
50. XDP
51. Pilot Run/LPC Debug/APS
52. EMI
53. Front_Panel
54. Front USB3.0
55. PCIe to PCI Bridge : TI XIO2001ZGU
56. Internal USB
57. Power Conn
58. Power Sequence
59. Power--> Linear 1
60. Power--> Linear 2
61. Power--> Linear 3
62. Power--> Vcore PWM
63. Power--> Vcore Driver
64. Power--> DDR Power
65. Power--> 5VSB / +3VDUAL
66. Power--> -12V

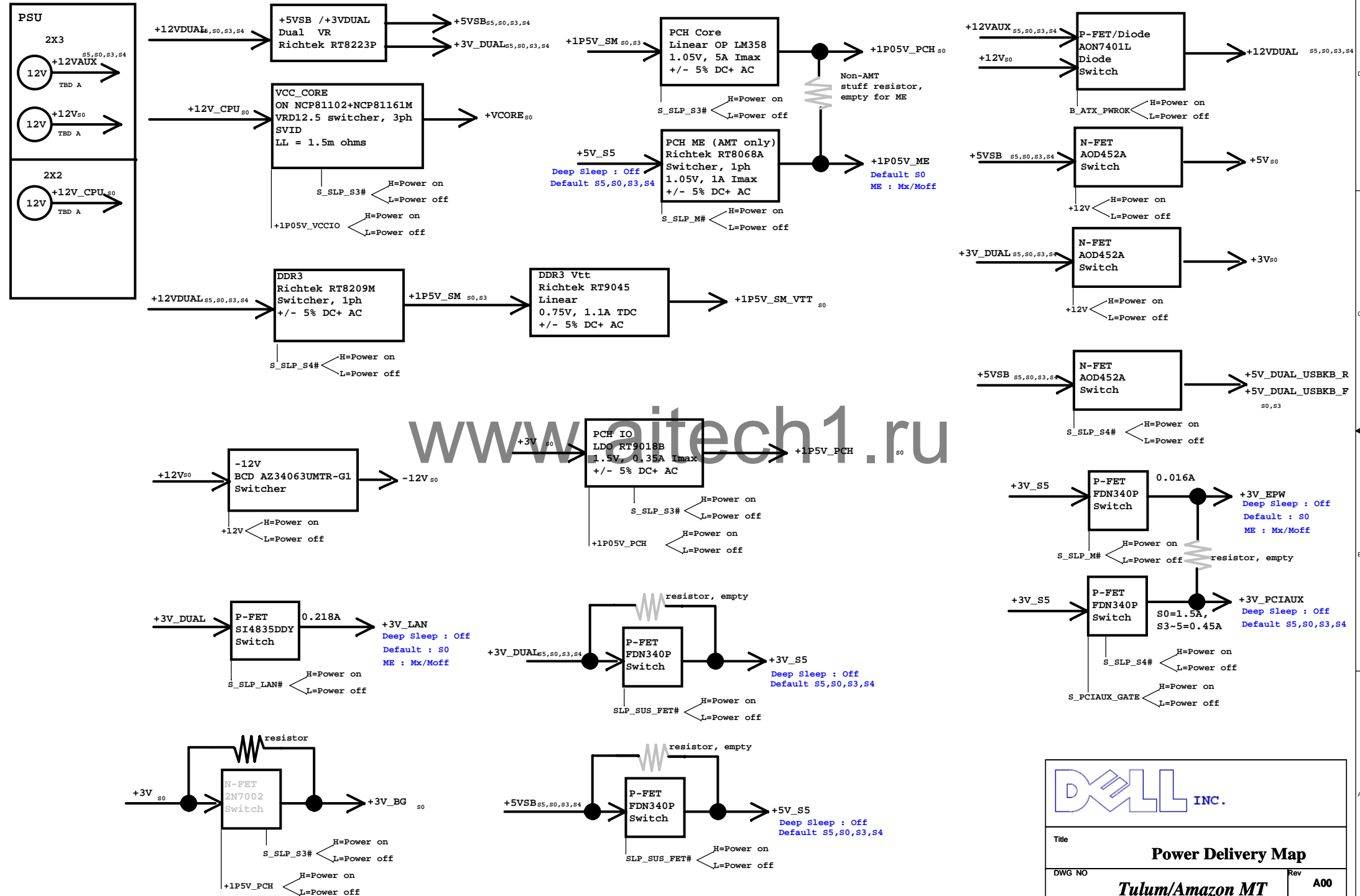


SMBUS DIAGRAM



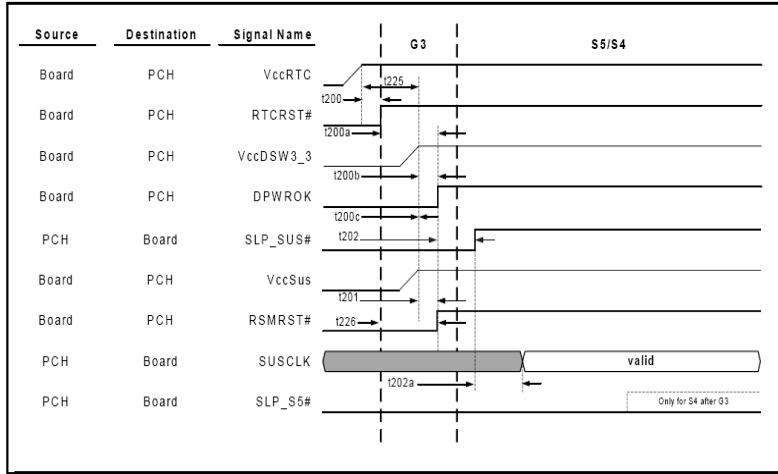


POWER DELIVERY MAP

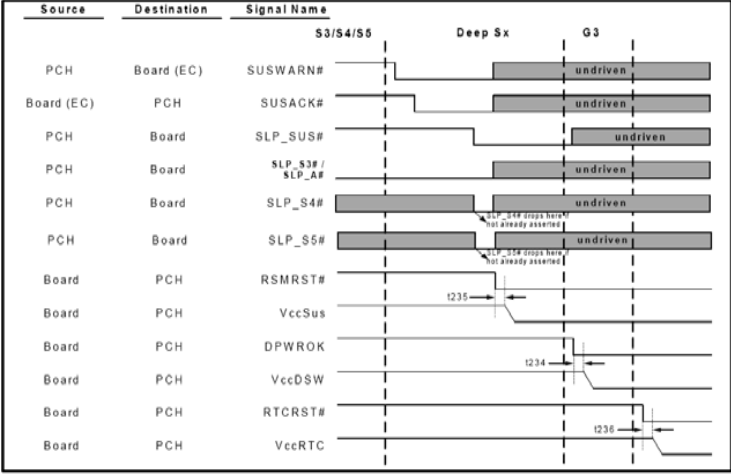


POWER ON Timing Diagram

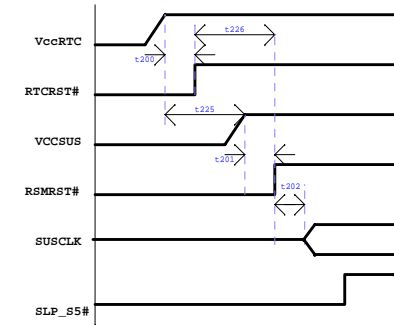
G3 --> S4/S5 (with Deep Sleep support)



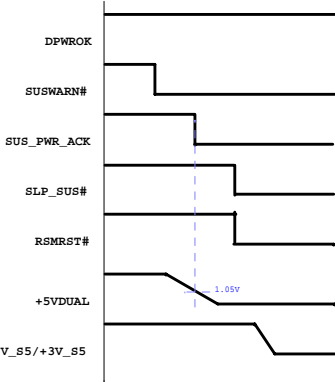
Sx --> Deep S4/S5 -->G3



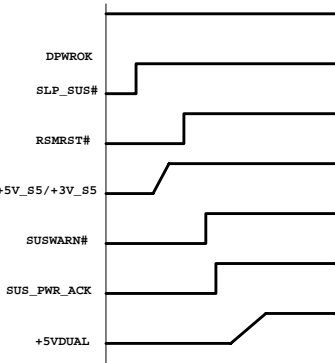
G3 to S4/S5 Timing Diagram



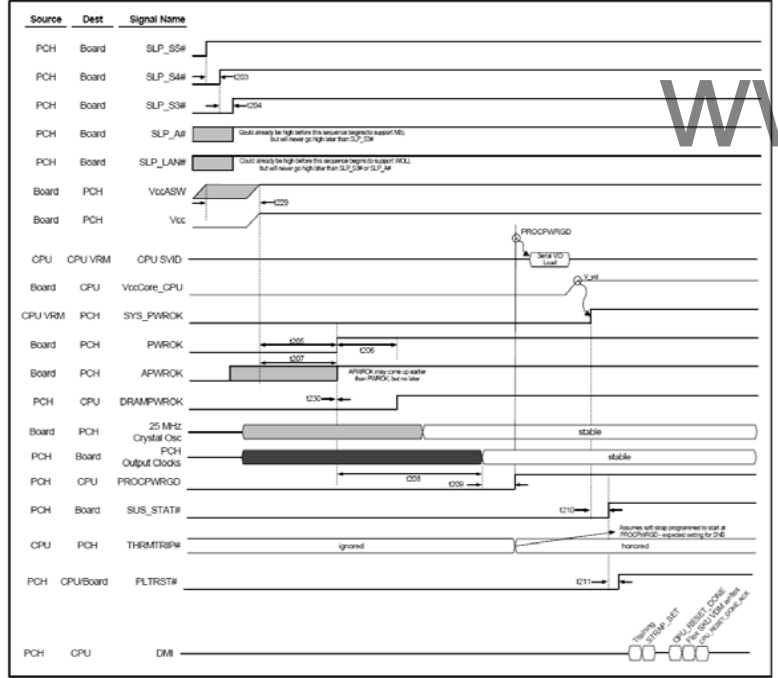
Deep Sleep Entry



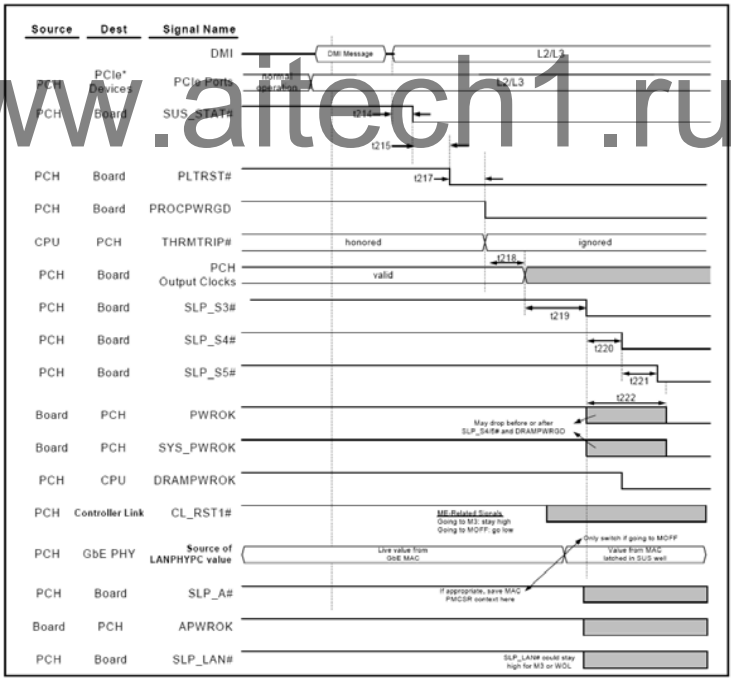
Deep Sleep Exit



S5 --> S0



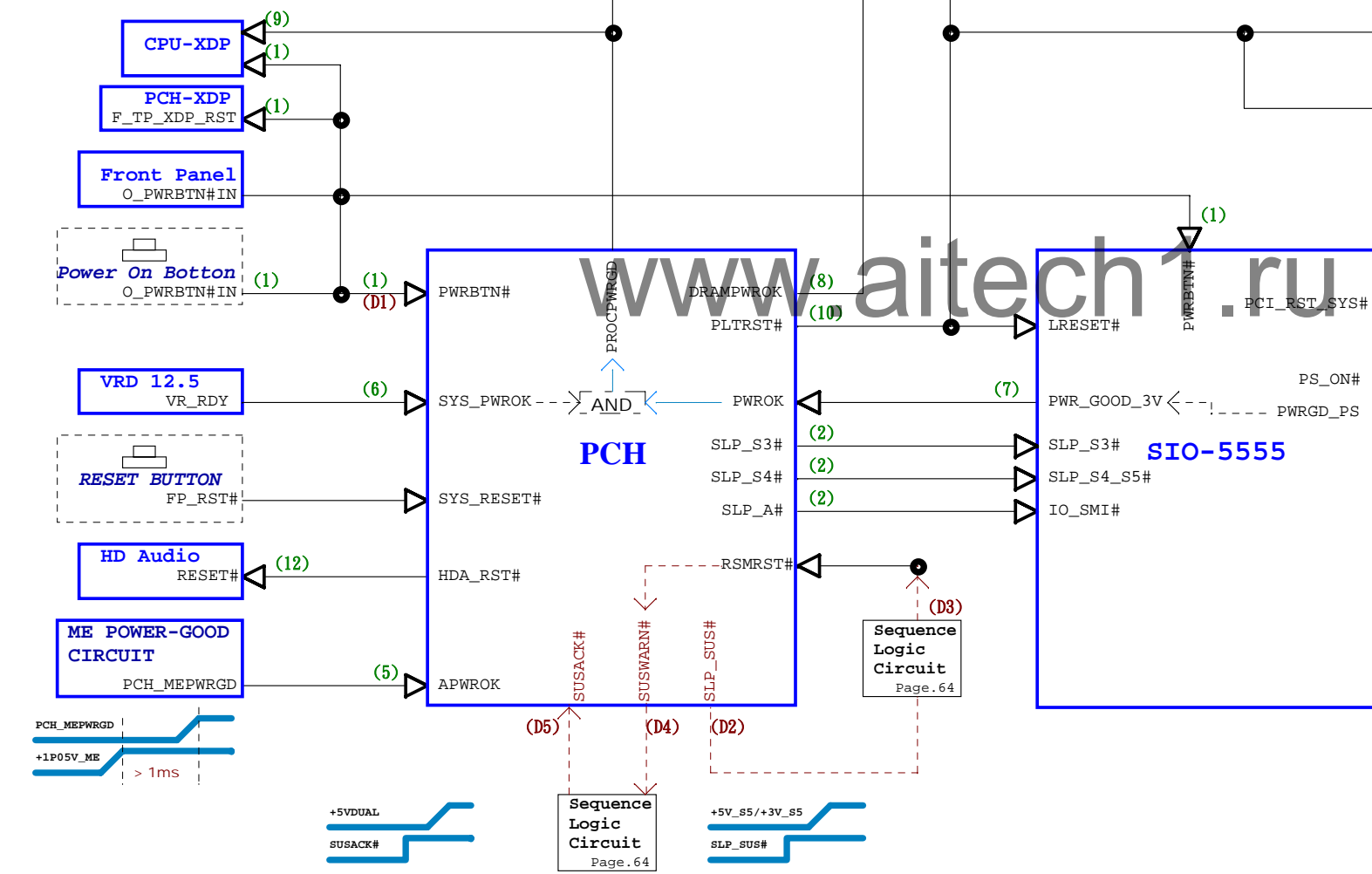
S0 --> S5



RESET / Power Good MAP

Sequence Signal Name:

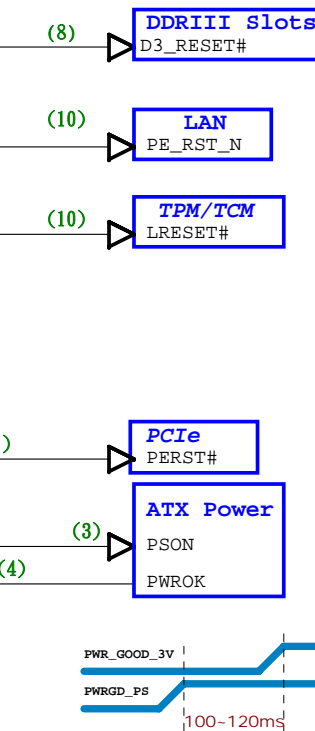
- (1) O_PWRBTN#IN
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PSON#
- (4) B_ATX_PWROK
- (5) PCH_MEPWRGD
- (6) S_PCH_SYSPWROK P_VR_READY
- (7) PWRGD_3V
- (8) H_DRAMPWRGD D3_RESET#
- (9) H_PWRGD
- (10) S_PLTRST# H_RESET#_R S_PLTRST#_R
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
- (12) A_Z_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O_PWRBTN#IN
- (D2) S_SLP_SUS#
- (D3) S_RSMRST#
- (D4) S_SUSWARN#
- (D5) S_SUS_PWR_ACK#



IRQ Routing Table

| | INTA# | INTB# | INTC# | INTD# | IDSEL | REQn# | GNTn# |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Slot3 | C | D | A | B | 18 | 0 | 0 |

STRAPPING Table

CPU side

| CFG[17:0] | Description | |
|-----------|--|--|
| [2] | PCI Express static x16 lane numbering reversal | 1: normal Default 0: lane numbers reversed |
| [6:5] | PCI Express Bifurcation | 00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default |

SIO SMSC5555

| PIN NAME | NET | | Strapping description |
|---------------------------------|-----------|---|---|
| GP070 / PWM4 (PIN127) | O_SPEAKER | 1 | Diag_En Disable |
| | | 0 | Diag_En Enable DEFAULT |
| DTR1# [TEST_EN] /GP051 (PIN104) | O_DTR1#_R | 1 | PE BOOT Loader Strap (DTR1#)= Load from SPI |
| | | 0 | PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT |

PCH

On-Die PLL Voltage Regulator Voltage Select

| HDA_SYNC | Description |
|----------|-------------|
| High | 1.5V |
| Low | 1.8V |

DEFAULT

On-Die PLL Voltage Regulator

| GPIO28 (IN-PU) | Description |
|----------------|------------------------|
| High | Regulator is enabled. |
| Low | Regulator is disabled. |

DEFAULT

Topblock Swap Mode

| GNT3#/GPIO55 (IN-PU) | Description |
|----------------------|-----------------------------|
| High | Topblock swap mode: Disable |
| Low | Topblock swap mode: Enable |

DEFAULT

No Reboot Mode

| SPKR (IN-PD) | Description |
|--------------|-------------------------|
| High | No reboot mode: Enable |
| Low | No reboot mode: Disable |

DEFAULT

Integrated 1.05V VRM

| INTVRMEN | Description |
|----------|-------------------------------|
| High | Integrated 1.05V VRM: Enable |
| Low | Integrated 1.05V VRM: Disable |

DEFAULT

TLS Confidentiality

| GPIO15 (IN-PD) | Description |
|----------------|--|
| High | ME Crypto TLS cipher suite with confidentiality |
| Low | ME Crypto TLS cipher suite with no confidentiality |

DEFAULT

Flash Descriptor Override Strap

| HDA_SDO | Description |
|---------|--|
| High | Flash descriptor security will be override |
| Low | Disable ME in Manufacturing Mode |

DEFAULT

DMI Rx Termination Voltage

| SPI_MOSI (IN-PD) | Description |
|------------------|----------------------------|
| Low | DMI Rx Termination Voltage |

DEFAULT

DMI Termination Voltage

| NV_CLE (IN-PU) | Description |
|----------------|---------------------------------------|
| High | DMI and FDI Tx/Rx Termination Voltage |

DEFAULT

Boot BIOS Destination Selection

| GNT1# (IN-PU) | SATA1GP/GP19 (IN-PU) | Description |
|---------------|----------------------|----------------------------|
| Low | Low | Flash cycle routed to LPC |
| High | Low | Flash cycle routed to PCI |
| Low | High | Flash cycle routed to NAND |
| High | High | Flash cycle routed to SPI |

DEFAULT

Deep S4/S5 Well on-die Voltage Regulator Enable

| DSWVRMEN | Description |
|----------|-------------|
| High | Enable |
| Low | Disable |

DEFAULT

Digital Port C Strap

| DDPC_CTRLDATA | Description |
|---------------|------------------|
| High | Configure Port C |
| Low | Disable |

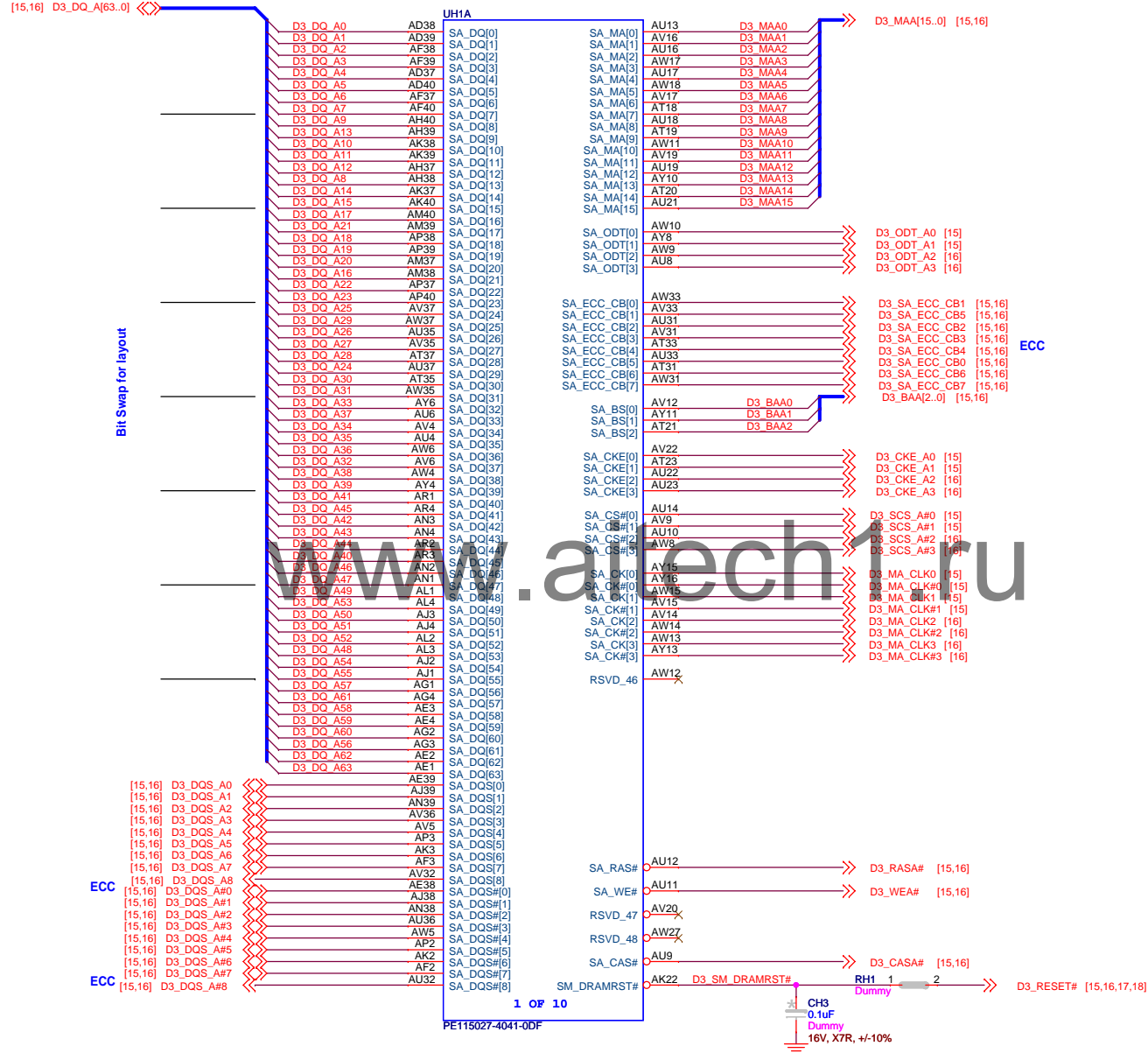
DEFAULT



Title
GPIO/IRQ/IDSEL Table

DWG NO
Tulum/Amazon MT

Rev
A00



| BIT SWIZZLE TABLE | | | |
|-------------------|------|-------|----|
| DDRO_DQ[8] | AH30 | DQ 9 | |
| DDRO_DQ[9] | AH39 | DQ 10 | 13 |
| DDRO_DQ[13] | AH38 | DQ 8 | 21 |
| DDRO_DQ[16] | AM40 | DQ 17 | 17 |
| DDRO_DQ[17] | AM39 | DQ 16 | 25 |
| DDRO_DQ[21] | AM38 | DQ 15 | 26 |
| DDRO_DQ[24] | AV37 | DQ 12 | 18 |
| DDRO_DQ[25] | AW37 | DQ 29 | |
| DDRO_DQ[29] | AU37 | AU37 | 24 |
| DDRO_DQ[32] | AV36 | DQ 33 | 33 |
| DDRO_DQ[33] | AV35 | DQ 32 | 37 |
| DDRO_DQ[37] | AV36 | DQ 32 | 32 |
| DDRO_DQ[40] | AR1 | DQ 41 | |
| DDRO_DQ[41] | AR4 | DQ 45 | |
| DDRO_DQ[45] | AR3 | DQ 40 | |
| DDRO_DQ[48] | AL1 | DQ 49 | |
| DDRO_DQ[49] | AL4 | DQ 53 | |
| DDRO_DQ[53] | AL3 | DQ 48 | |
| DDRO_DQ[56] | AG1 | DQ 57 | |
| DDRO_DQ[57] | AG4 | DQ 56 | |
| DDRO_DQ[61] | AG3 | DQ 61 | |
| DDRO_DQ[64] | AW33 | DQ 65 | |
| DDRO_DQ[65] | AV33 | DQ 69 | |
| DDRO_DQ[69] | AU33 | DQ 64 | |



| | |
|-------|------------------------|
| Title | CPU-1: DDR3_CHA |
|-------|------------------------|

| | | | |
|--------|-------------------------------|-----|------------|
| DWG NO | <i>Tulum/Amazon MT</i> | Rev | A00 |
|--------|-------------------------------|-----|------------|

Date: Tuesday, January 29, 2013 Sheet 9 of 66

[17,18] D3_DQ_B[63..0] <<>>



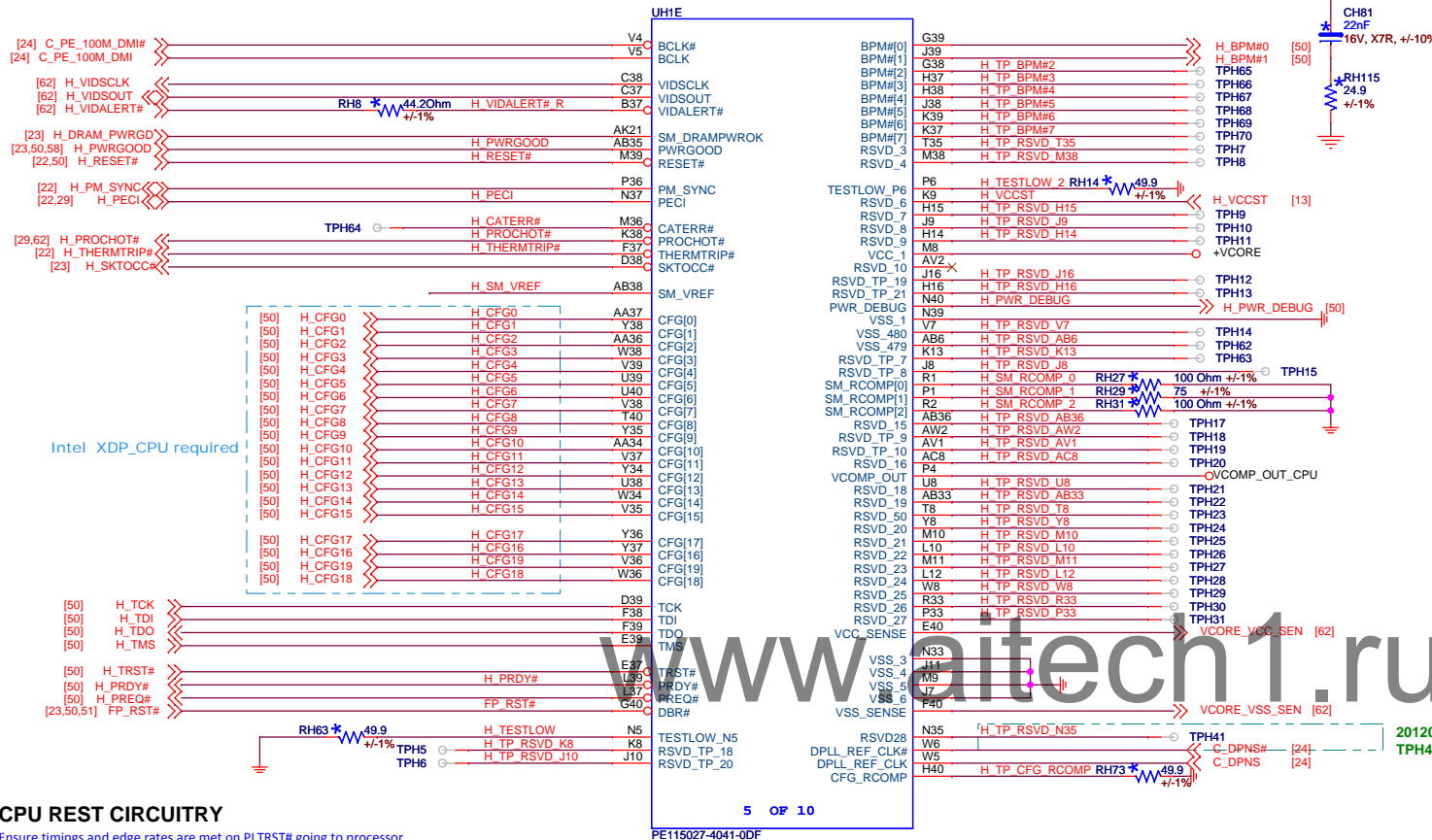
| |
|--------|
| DWG NO |
|--------|

Rev

Date: Tuesday, January 29, 2013

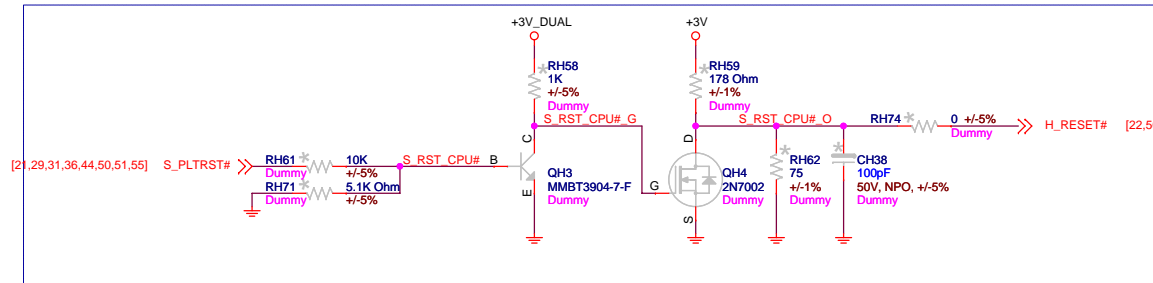
Sheet 10 of 66

MCP - VID,CTRL, MSIC



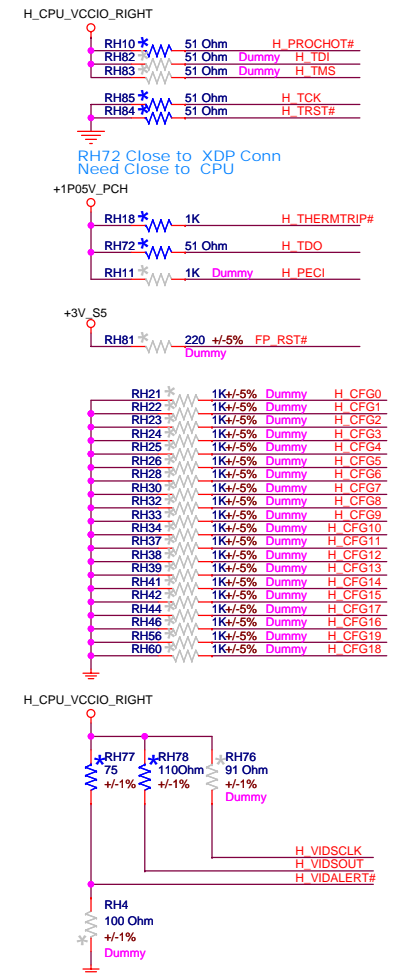
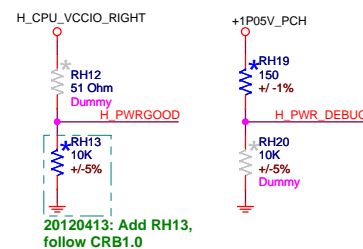
CPU REST CIRCUITRY

Ensure timings and edge rates are met on PLTRST# going to processor.

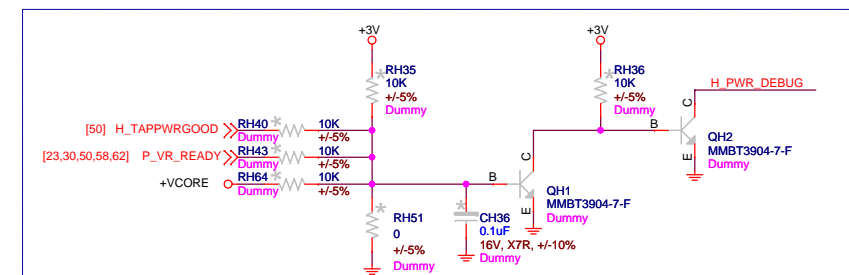


Check with Intel for this circuit necessary ??

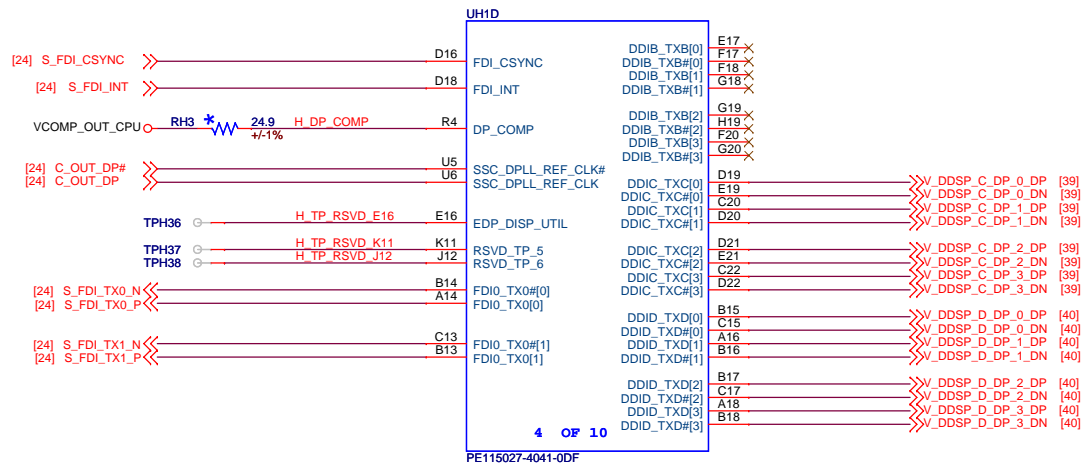
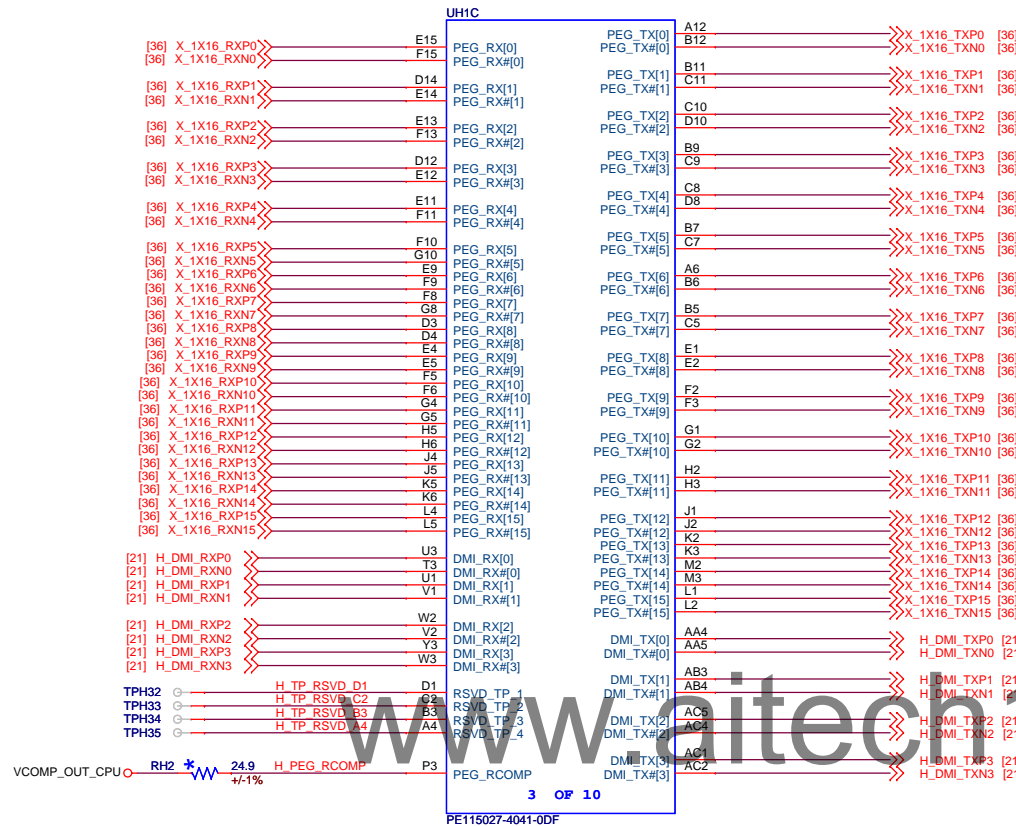
If RS71 pop, CPU RESET CIRCUIT need to Dummy



Check with Intel for this circuit necessary ??




| | | | |
|-----------------|---------------------------|-------|----------|
| Title | | | |
| CPU-3: VID/MISC | | | |
| DWG NO | Rev | | |
| Tulum/Amazon MT | | A00 | |
| Date: | Tuesday, January 29, 2013 | Sheet | 11 of 66 |

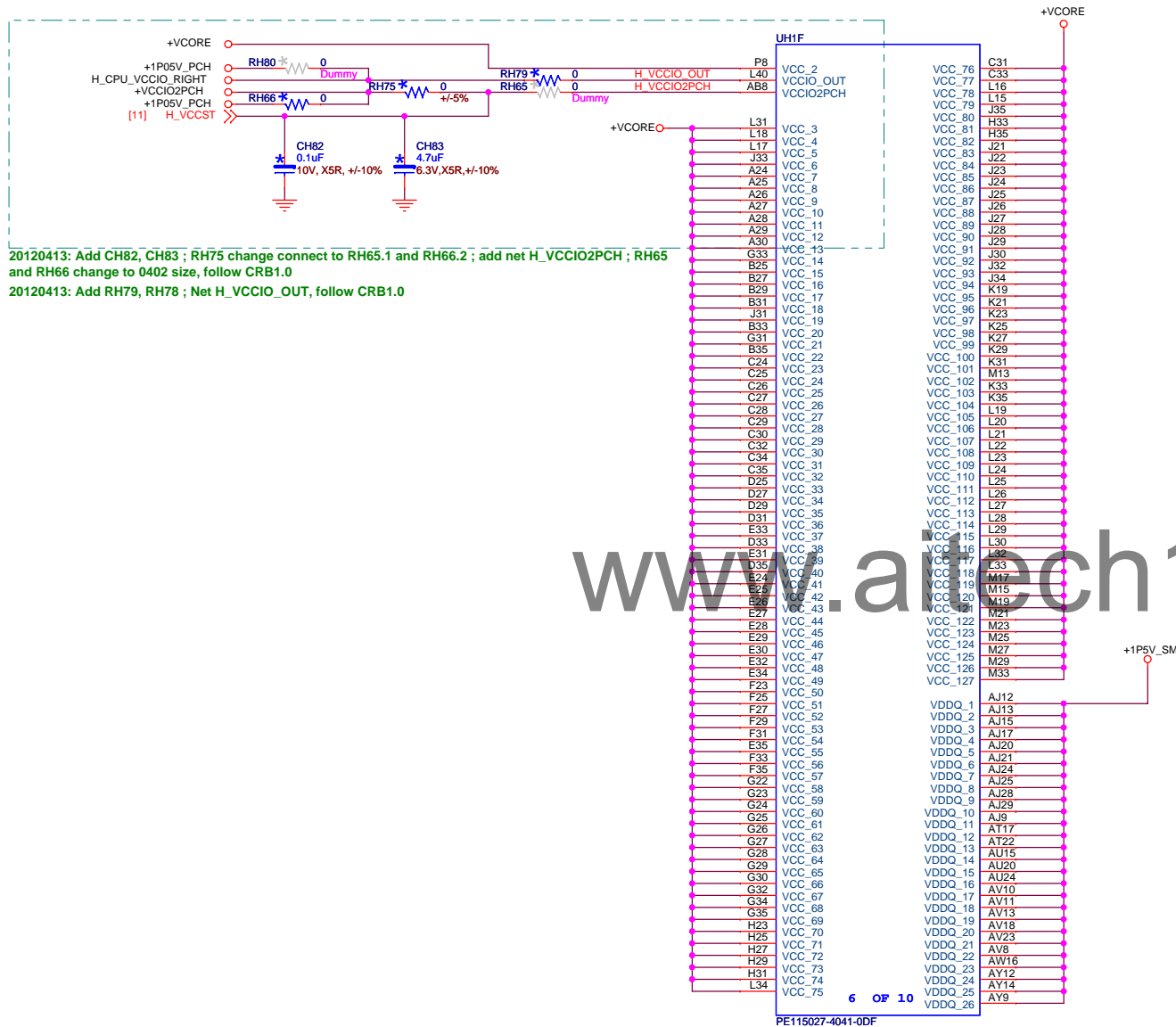


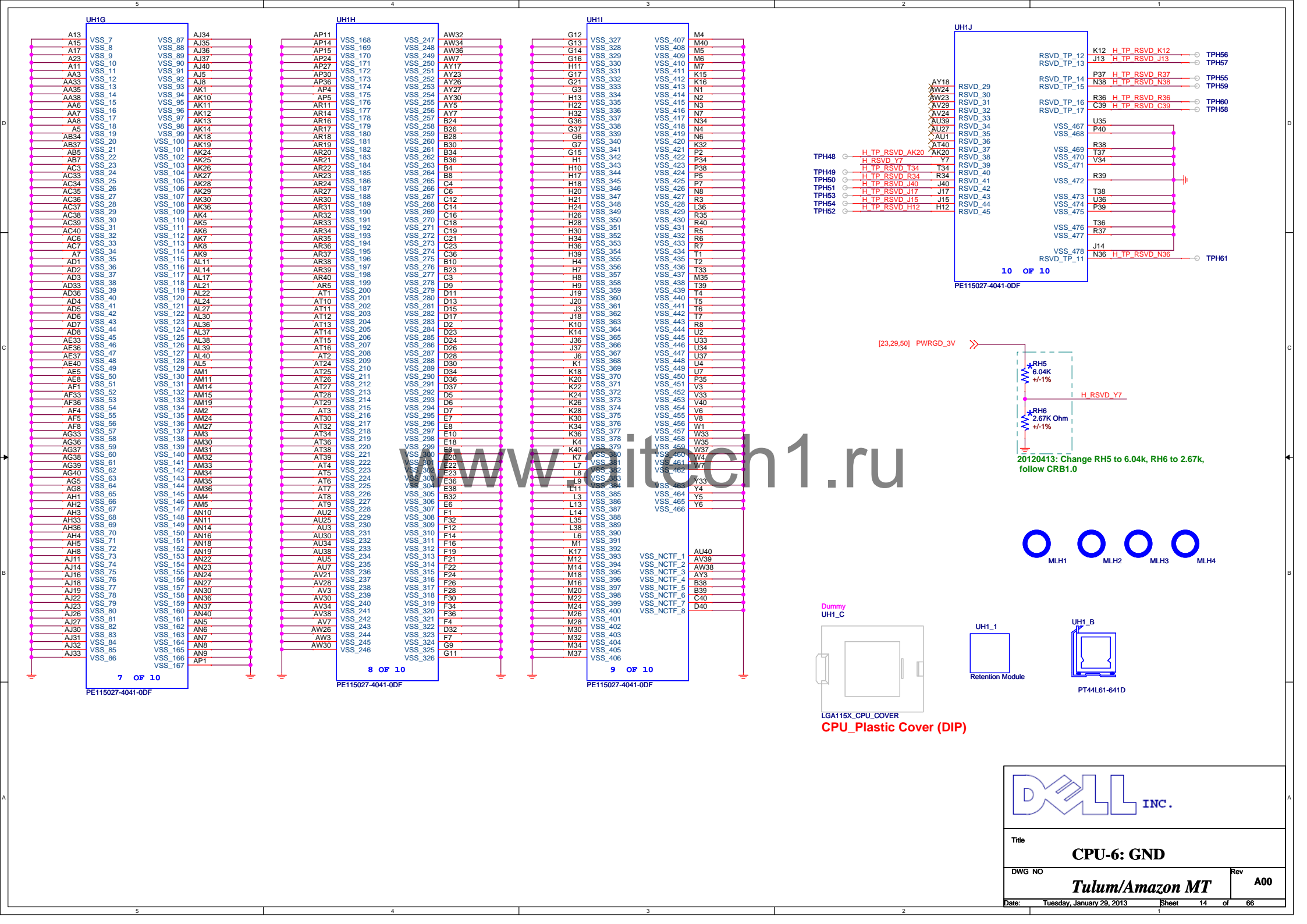
For Thunderbolt display .

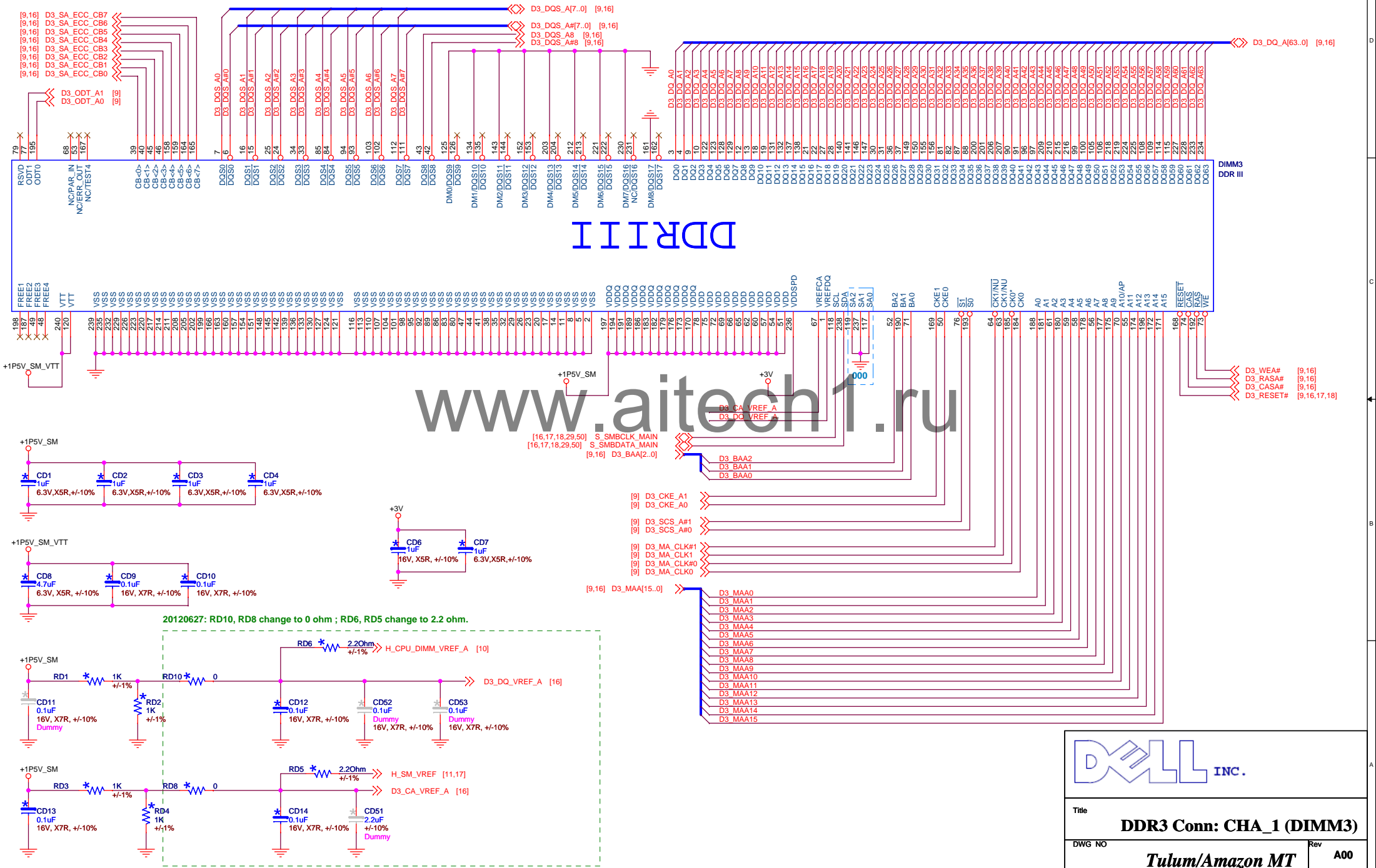
Display Port1

Display Port2

| | | |
|---|---------------------------|----------------|
|  | | |
| Title | | |
| CPU-4: FDI/PCIe/DMI/DP | | |
| DWG NO | | Rev |
| | Tulum/Amazon MT | A00 |
| Date: | Tuesday, January 29, 2013 | Sheet 12 of 66 |

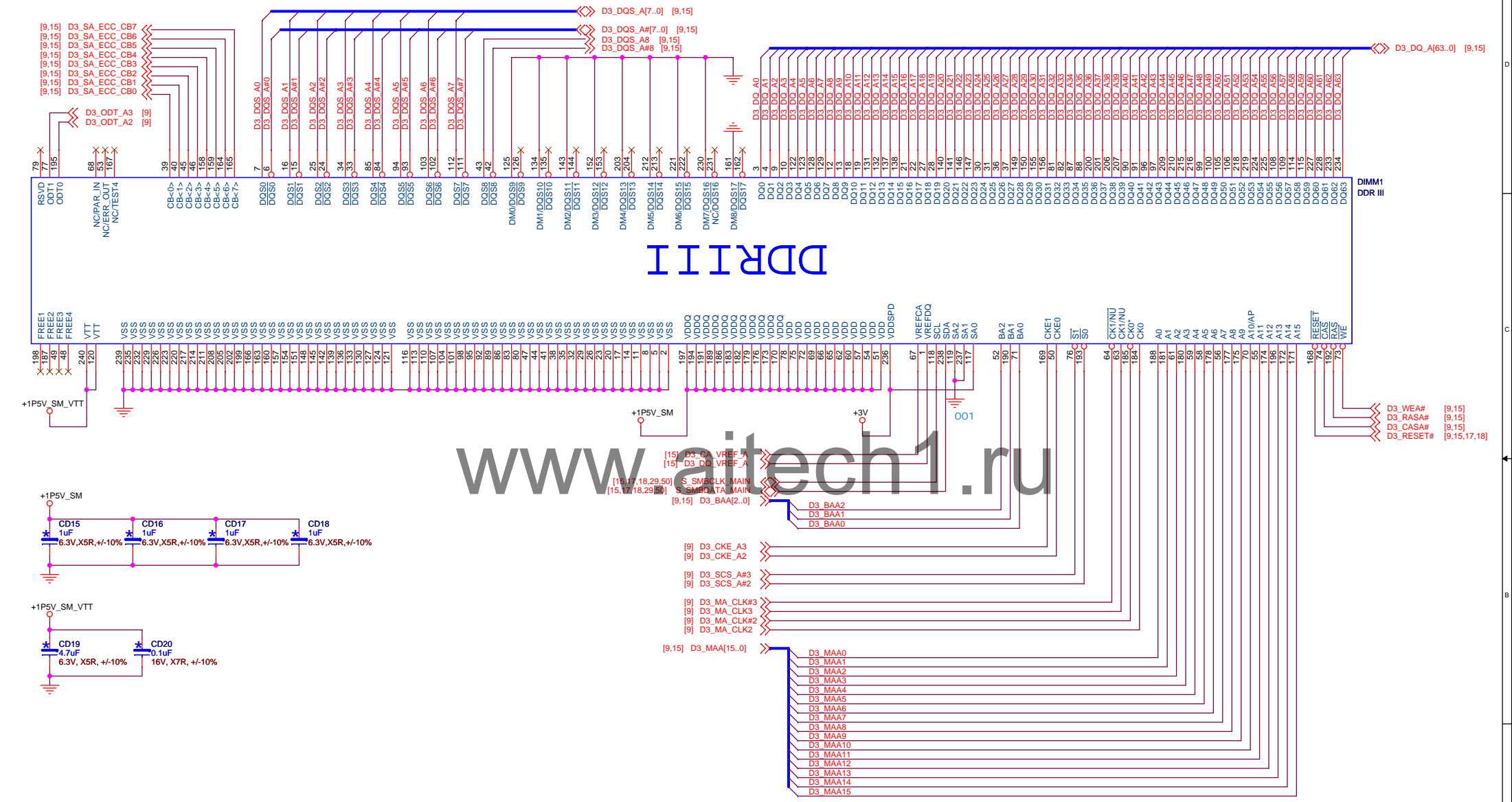






Title **DDR3 Conn: CHA_1 (DIMM3)**

| | |
|-------------------------------|------------|
| DWG NO | Rev |
| <i>Tulum/Amazon MT</i> | A00 |





INC.

Title

DDR3 Conn: CHA_2 (DIMM1)

DWG NO

Tulum/Amazon MT

Rev

A00

Date:

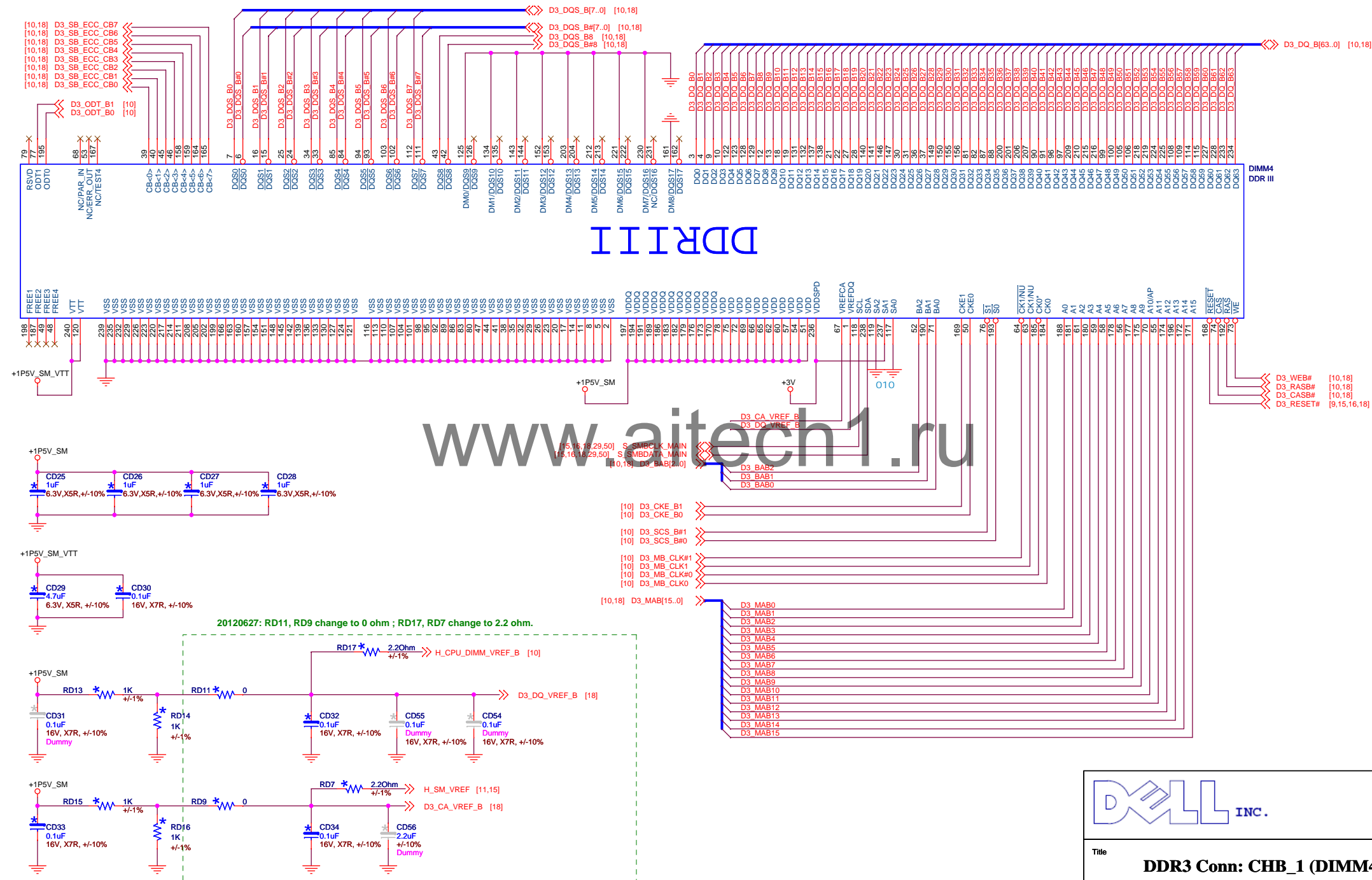
Tuesday, January 29, 2013

Sheet

16

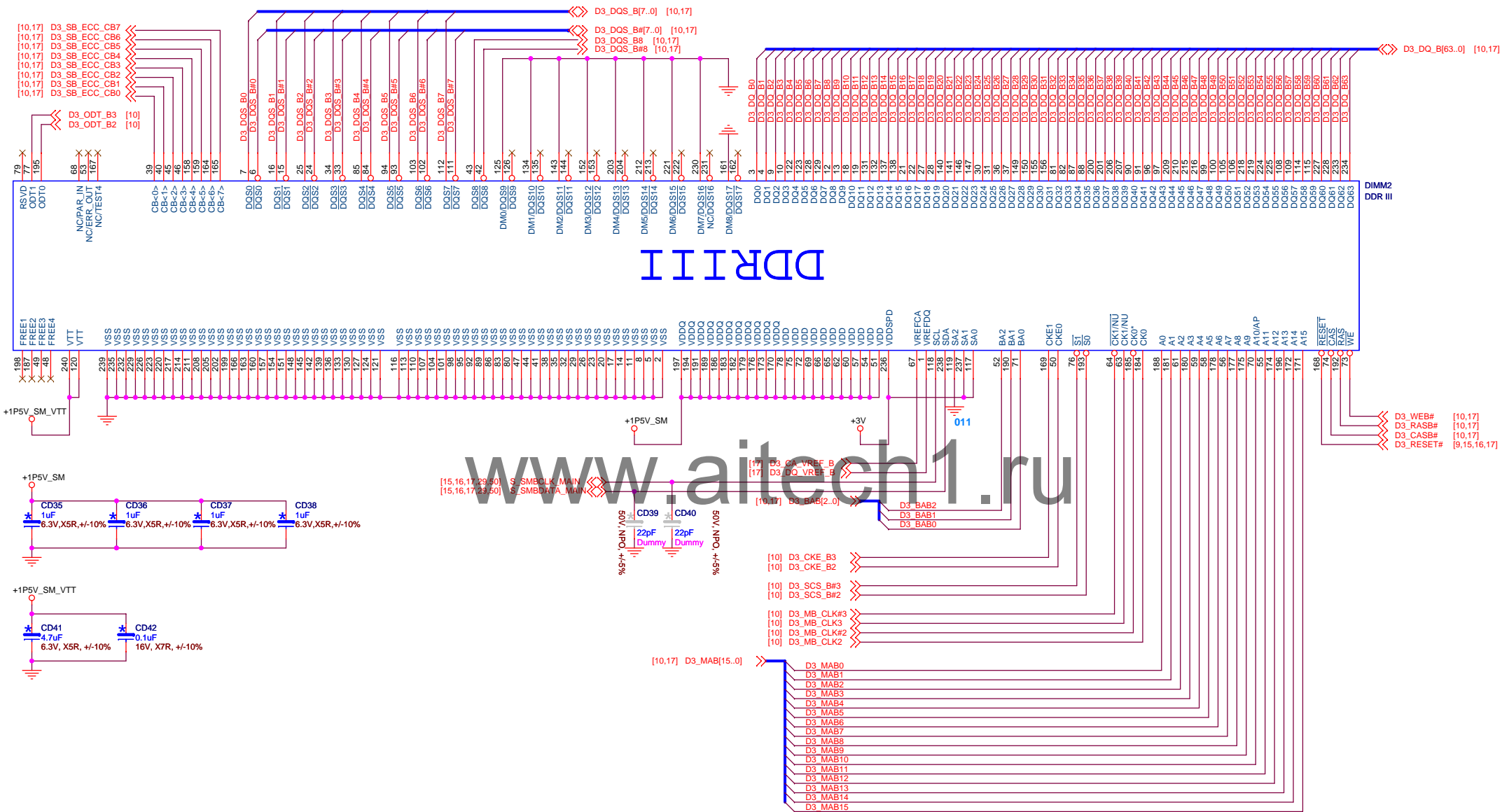
of

66



| | |
|-------|--------------------------|
| Title | DDR3 Conn: CHB_1 (DIMM4) |
|-------|--------------------------|

| | |
|------------------------|------------|
| DWG NO | Rev |
| Tulum/Amazon MT | A00 |




Title **DDR3 Conn: CHB_2 (DIMM2)**

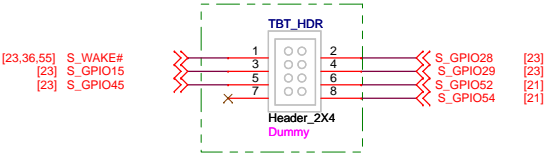
| | |
|------------------------|------------|
| DWG NO | Rev |
| <i>Tulum/Amazon MT</i> | A00 |

<LBL>
2D-Label
Lable

www.aitech1.ru

| | | |
|---|-------------------------------|-------------------|
|  | | |
| Title Label | | |
| DWG NO | <i>Tulum/Amazon MT</i> | Rev A00 |
| Date: | Tuesday, January 29, 2013 | Sheet 19 of 66 |

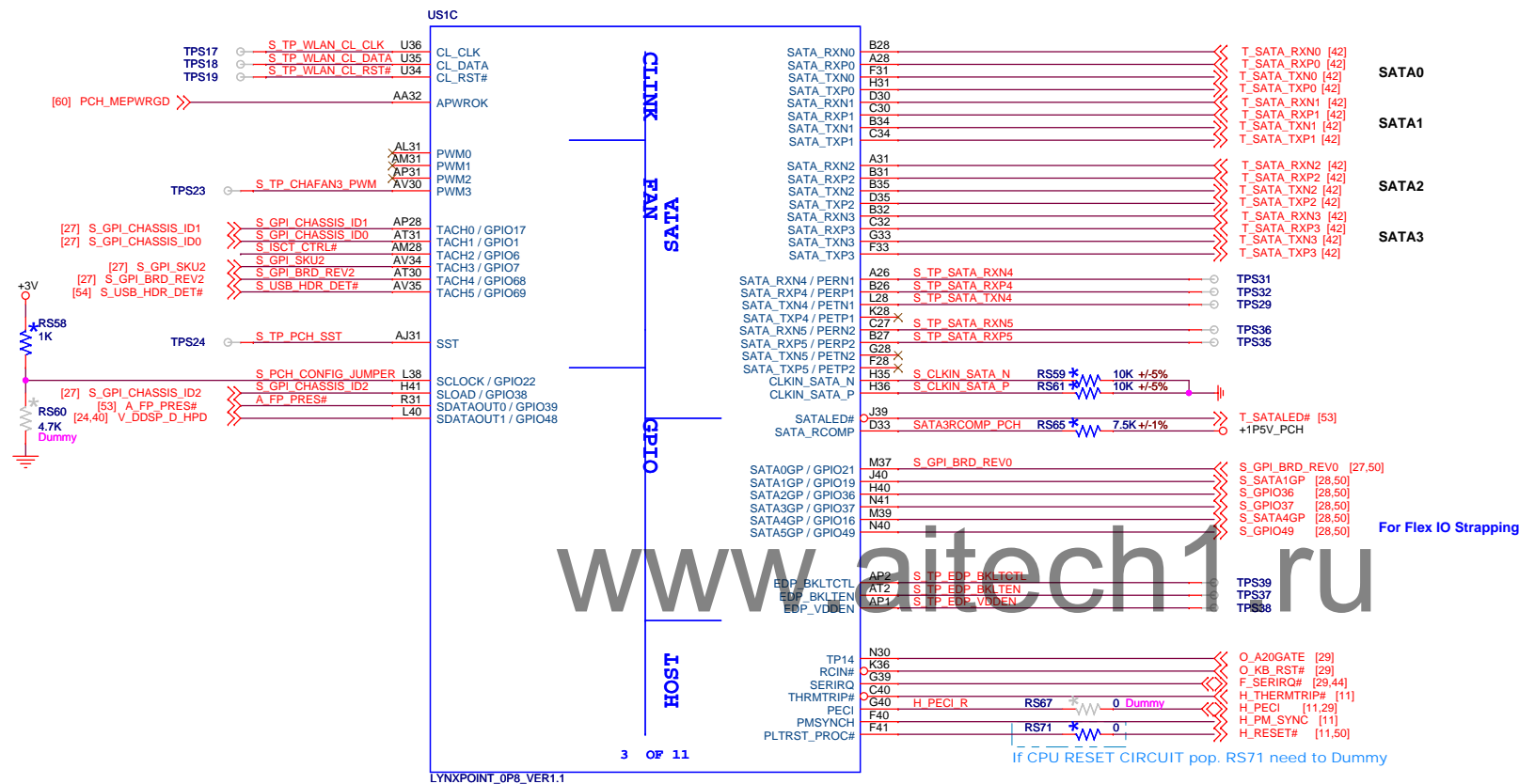
20120626: Add TBT_HDR
20120703: TBT_HDR compoment
REMARK cahnge to Remark



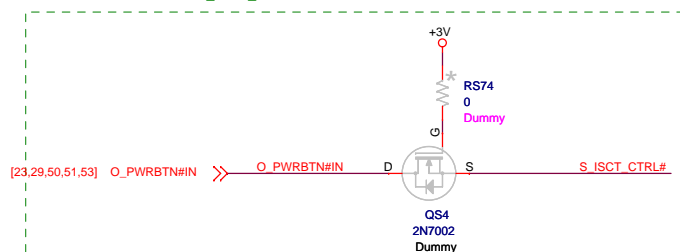
www.aitech1.ru



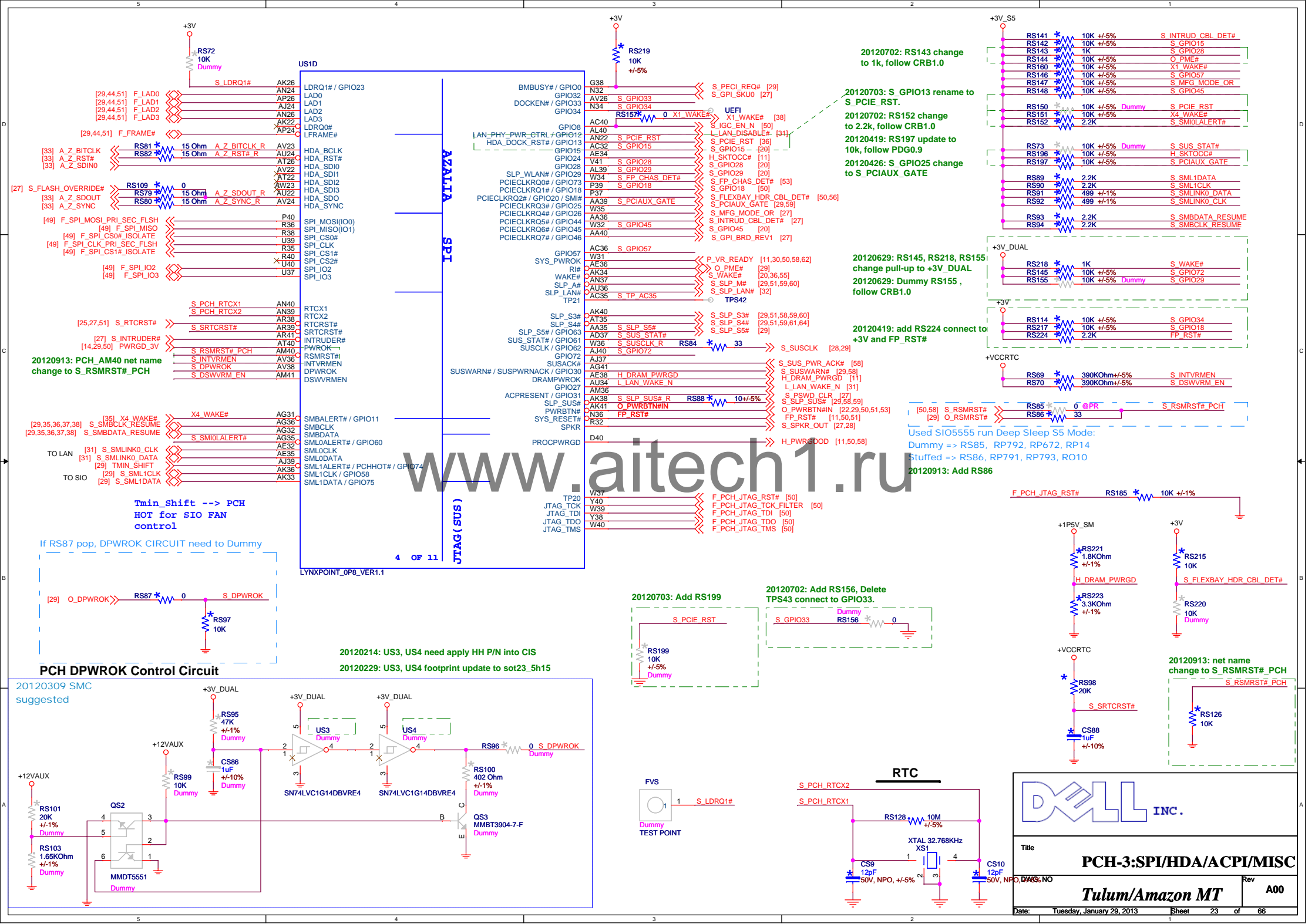
| | | | |
|--------|---------------------------|----------|---------|
| Title | | TBT_HDR | |
| DWG NO | Tulum/Amazon MT | | Rev A00 |
| Date: | Tuesday, January 29, 2013 | Sheet 20 | of 66 |



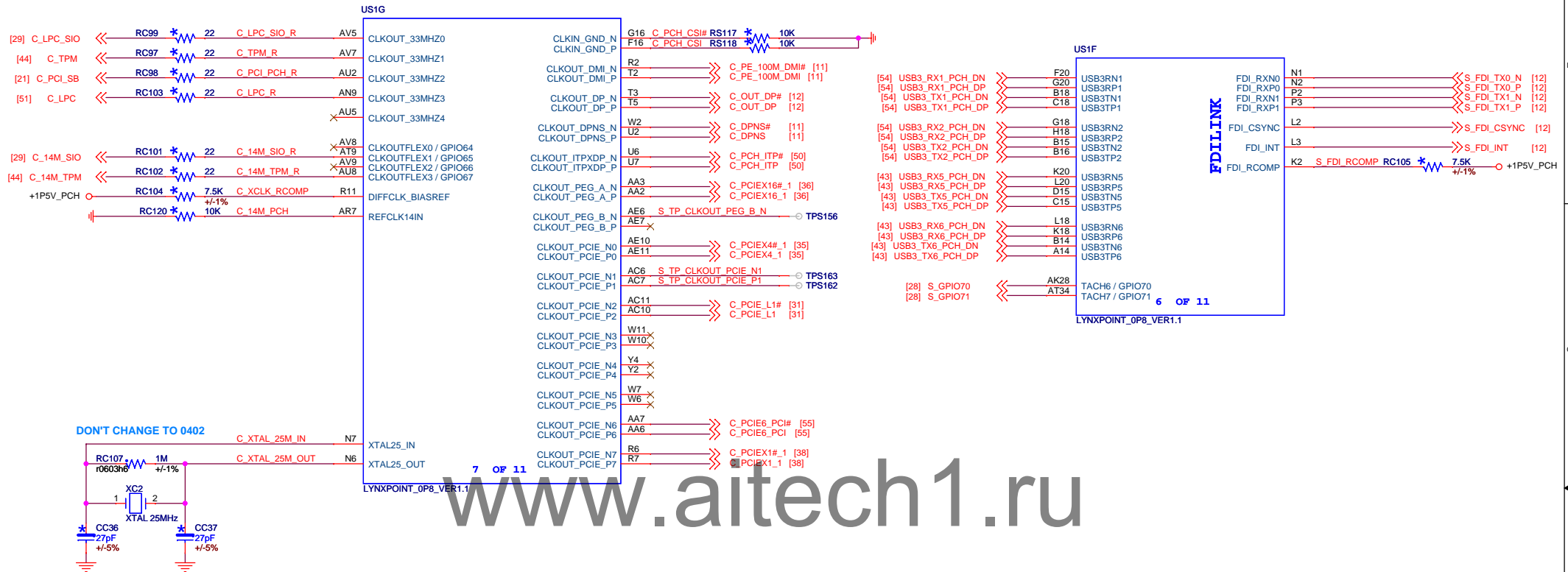
20120625: Add QS4 and S_ISCT_CTRL#



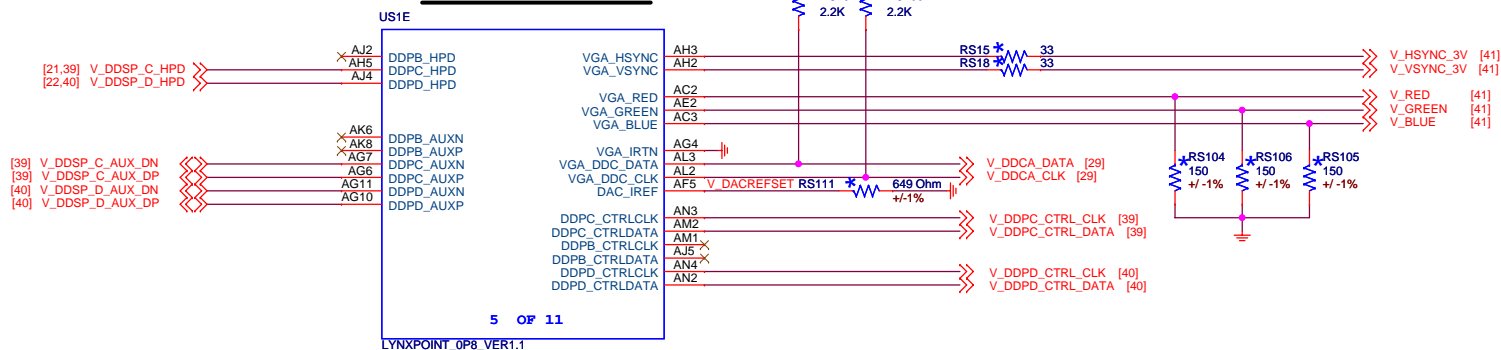
| | |
|---------------------------------|----------------|
| | |
| | |
| Title | |
| PCH-2: SATA/HOST/GPIO | |
| DWG NO | Rev |
| Tulum/Amazon MT | A00 |
| Date: Tuesday, January 29, 2013 | Sheet 22 of 66 |



PCH - CLOCK DISTRIBUTION



PCH - DP AND RGB



DELL INC.

Title

PCH-4: VGA/USB3/CLK/FDI

DWG NO

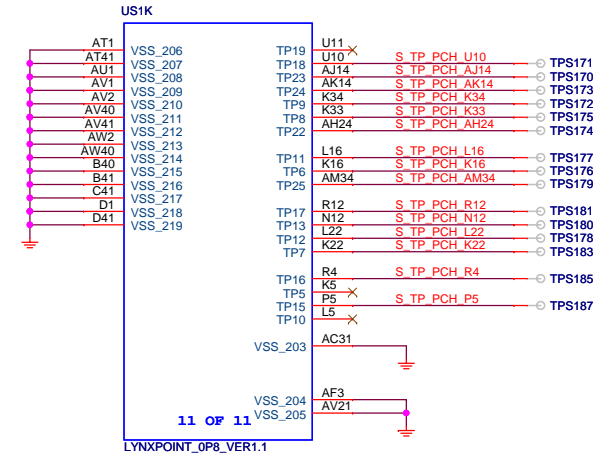
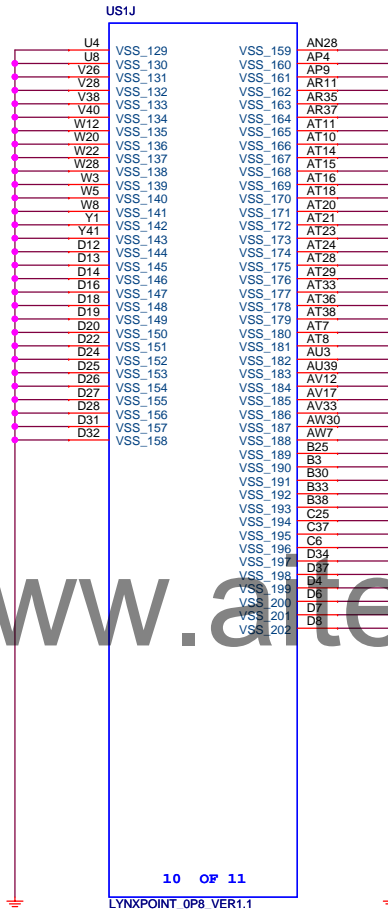
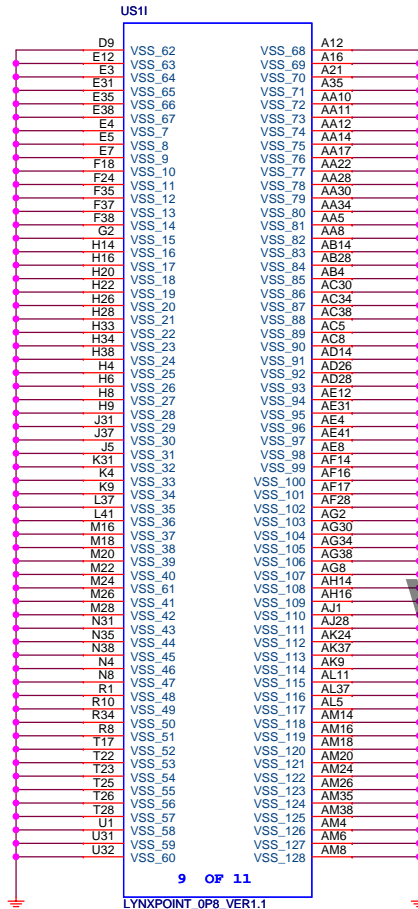
Tulum/Amazon MT

Rev

A00

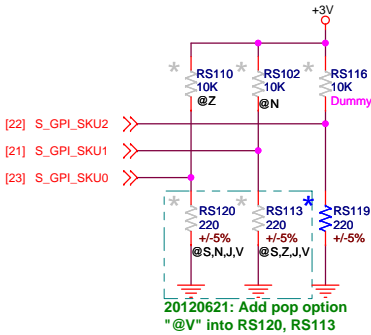
Date: Tuesday, January 29, 2013

Sheet 24 of 66

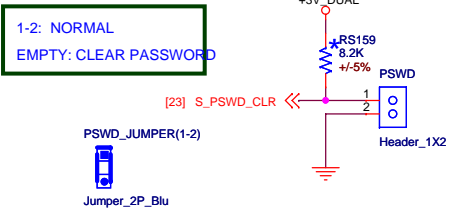


SKU ID

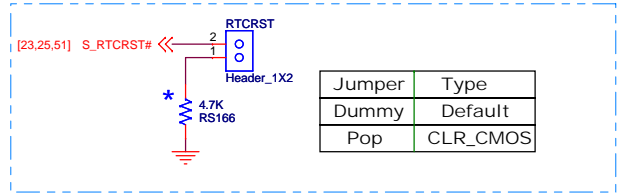
| SKU1 | SKU0 | Type |
|------|------|---------------|
| 0 | 0 | TPM |
| 0 | 1 | TCM |
| 1 | 0 | NO TPM/NO TCM |
| 1 | 1 | Reserved |



Clear Password

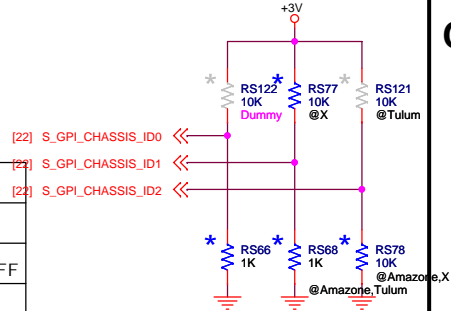


CLR_CMOS

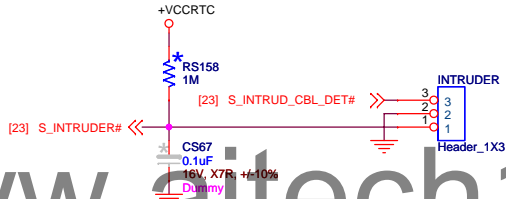


Chassis ID

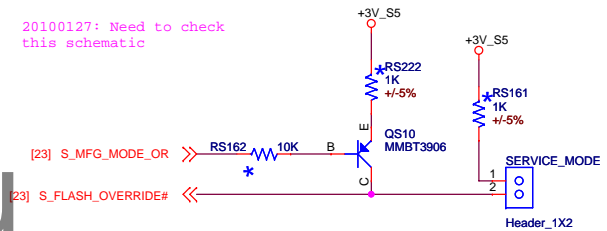
| ID2 | ID1 | ID0 | Type |
|-----|-----|-----|-----------|
| 1 | 0 | 1 | SFF |
| 1 | 1 | 0 | Tulum SFF |
| 1 | 1 | 1 | X-SFF |
| 0 | 0 | 0 | MT |
| 1 | 0 | 0 | Tulum MT |
| 0 | 1 | 0 | X-MT |
| 0 | 1 | 1 | USFF |



Chassis Intruder

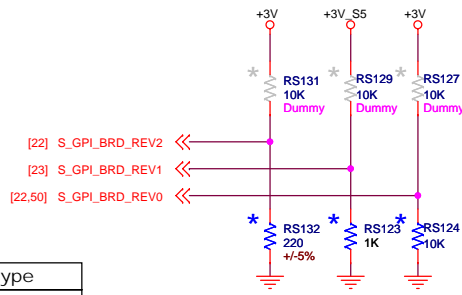


ME Disable (Flash override)

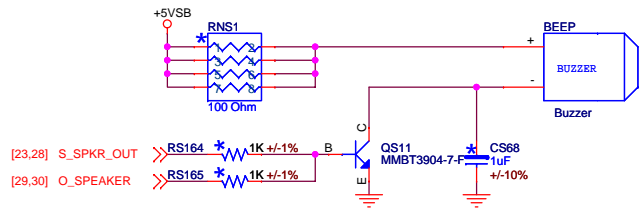


BOARD ID

| Rev2 | Rev1 | Rev0 | Type |
|------|------|------|----------|
| 0 | 0 | 0 | Default |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |



BEEP



Title

PCH-8: MISC CONN/BEEP/ID

DWG NO

Tulum/Amazon MT

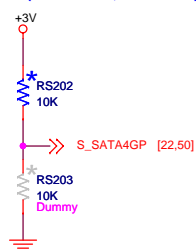
Rev

A00

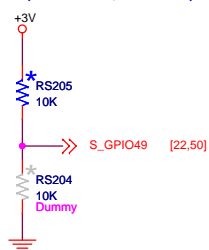
Date: Tuesday, January 29, 2013

Sheet 27 of 66

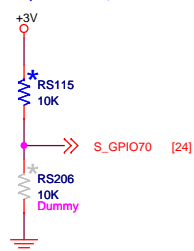
GPIO16 (H-->SATA4 ; L-->PCle1)



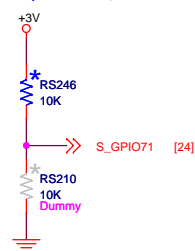
GPIO49 (H-->SATA5 ; L-->PCle2)



GPIO70 (H-->PCle1 ; L-->USB3 3)

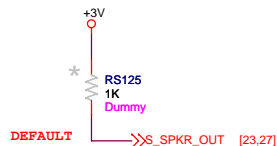


GPIO71 (H-->PCle2 ; L-->USB3 4)



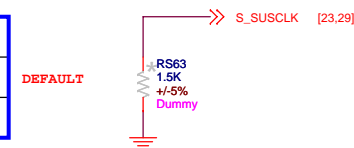
No Reboot Mode

| SPKR (IN-PD) | Description |
|--------------|-------------------------|
| High | No reboot mode: Enable |
| Low | No reboot mode: Disable |



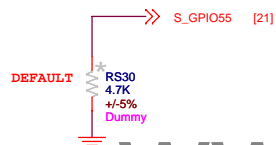
On-Die PLL Voltage Regulator

| GPIO62/SUSCLK (IN-PU) | Description |
|-----------------------|------------------------|
| High | Regulator is enabled. |
| Low | Regulator is disabled. |



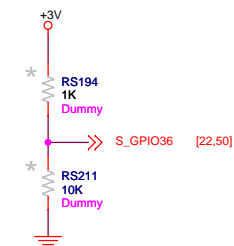
Topblock Swap Mode

| GPIO55 (IN-PU) | Description |
|----------------|-----------------------------|
| High | Topblock swap mode: Disable |
| Low | Topblock swap mode: Enable |



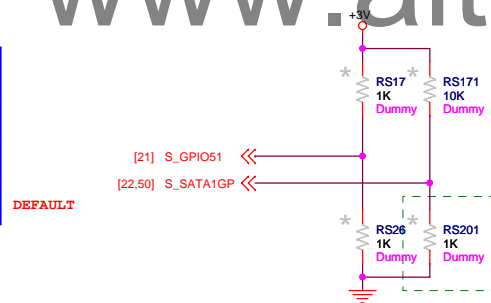
DMI Rx Termination

| GPIO36 (IN-PD) | Description |
|----------------|----------------------------|
| Low | DMI Rx Termination Voltage |



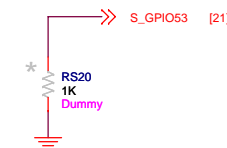
Boot BIOS Destination Selection

| GPIO51 (IN-PU) | SATA1GP/GP19 (IN-PU) | Description |
|----------------|----------------------|---------------------------|
| Low | Low | Flash cycle routed to LPC |
| High | Low | Flash cycle routed to PCI |
| High | High | Flash cycle routed to SPI |



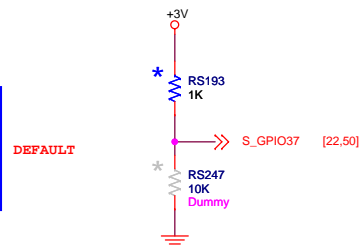
20120524: RS201 change to 1k, follow PDG1.0

DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW



TLS Confidentiality

| GPIO37 (IN-PD) | Description |
|----------------|--|
| High | ME Crypto TLS cipher suite with confidentiality |
| Low | ME Crypto TLS cipher suite with no confidentiality |



Title

PCH-9: STRAP OPTION

DWG NO

Tulum/Amazon MT

Rev

A00

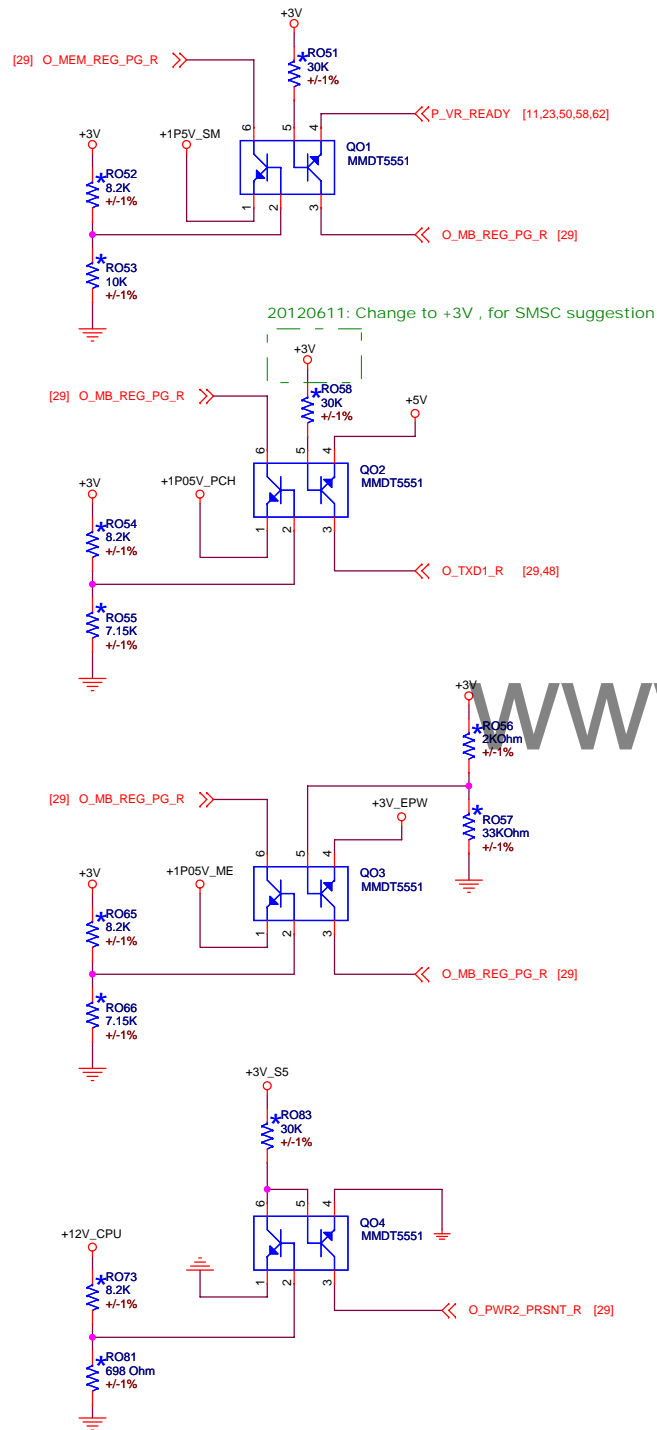
Date: Tuesday, January 29, 2013

Sheet 28 of 66

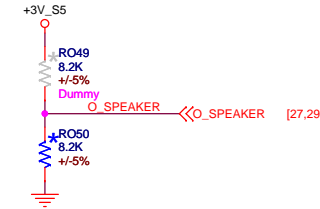
20120502: UO1 change to
SCH555-NS B. version B.



5555 PRE-POST DIAG Monitor



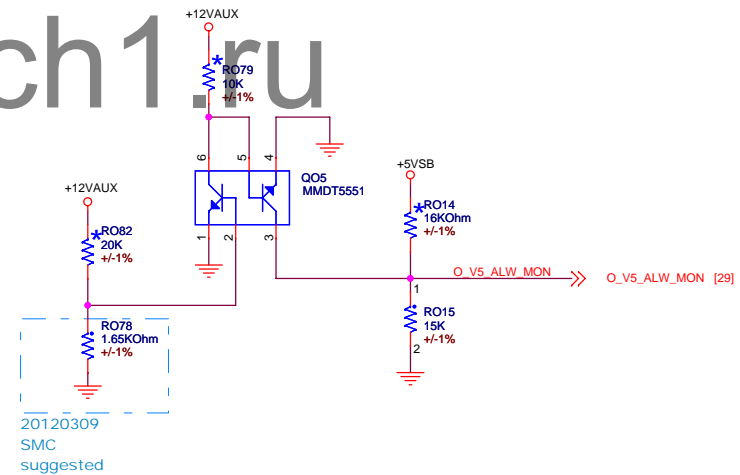
SIO STRAPING



SIO STRAPING

| | SPEAKER | |
|-----------|---------|--|
| | Diag_En | |
| PULL HIGH | Disable | |
| PULL LOW | Enable | |

SIO5555 V5_ALW Monitor

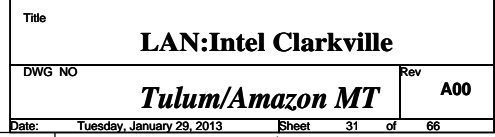
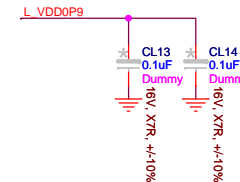


| | | |
|---------------------------------|-----------------|---------|
| | | |
| Title | | |
| SIO-SCH5555-2 | | |
| DWG NO | Tulum/Amazon MT | Rev A00 |
| Date: Tuesday, January 29, 2013 | Sheet 30 | of 66 |

Intel Clarkville

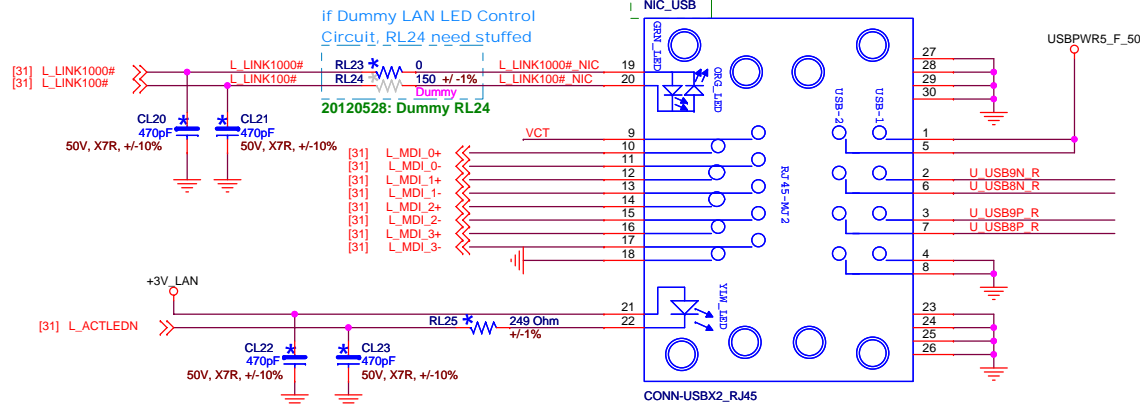


Schematic diagram of the L_LAN_DISABLE# signal line. The signal line is red and labeled "L_LAN_DISABLE# R". It is connected to a 3V_LAN supply through a 10K resistor (RL10) and to ground through a 10K resistor (RL14). Both resistors are labeled "Dummy". A blue resistor (RL27) is connected to the signal line and to a blue triangle symbol labeled "[23] L_LAN_DISABLE#". The signal line is also connected to a blue triangle symbol labeled "0".



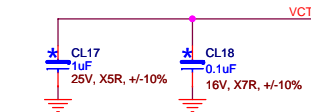
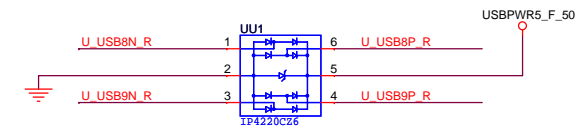
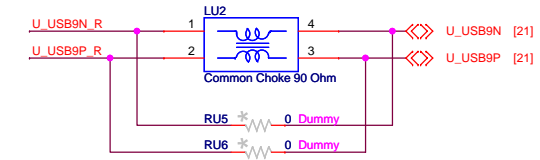
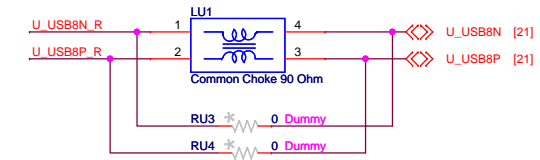
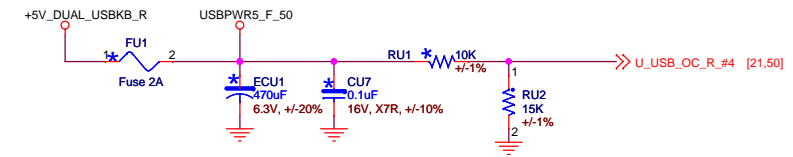
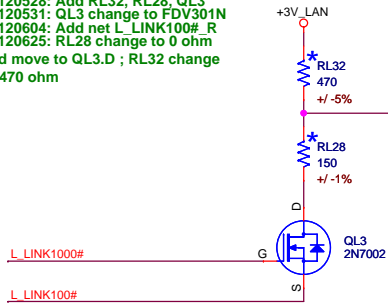
LAN CONNECTOR

20120214: NIC_USB need apply HH P/N into CIS
20120217: NIC_USB Change to JFM38U1B-21M5-4F , need apply HH P/N into CIS
20120229: NIC_USB Change to JFM38U1B-21M5-4F, link from M disk

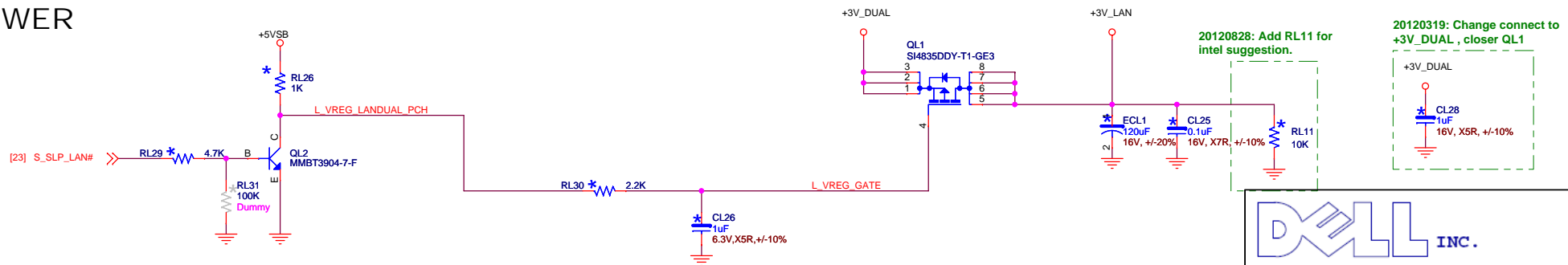


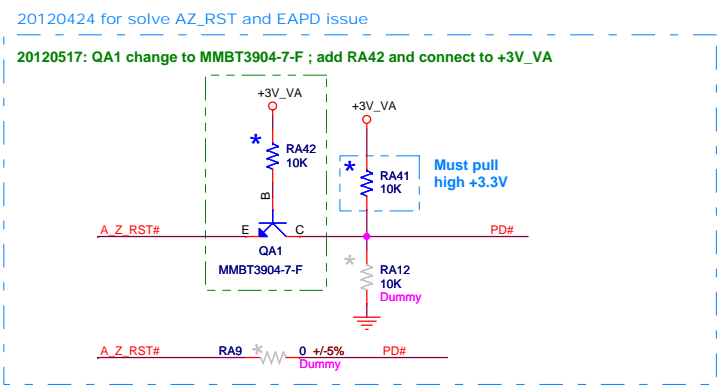
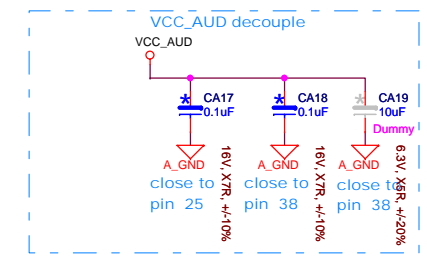
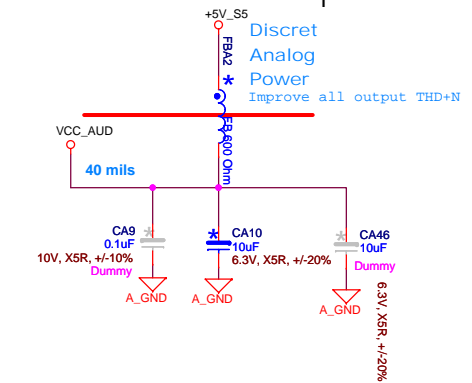
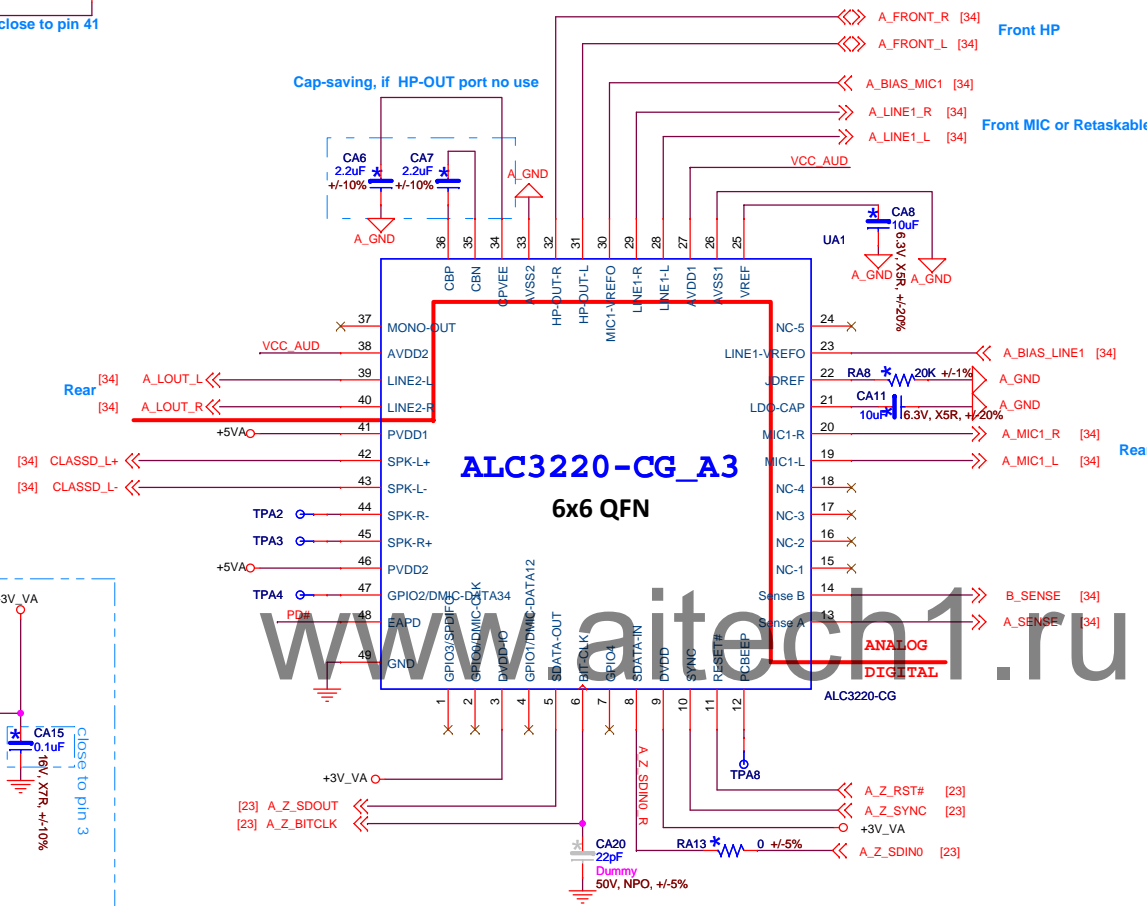
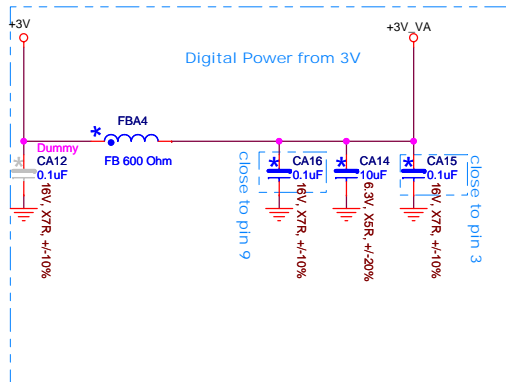
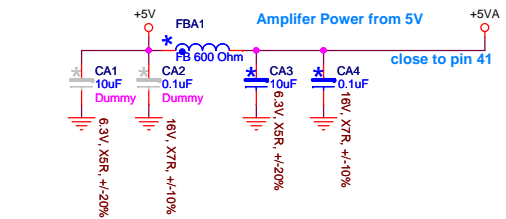
LAN LED Control Circuit

20120528: Add RL32, RL28, QL3
20120531: QL3 change to FDV301N
20120604: Add net L_LINK100#_R
20120625: RL28 change to 0 ohm
and move to QL3.D ; RL32 change
to 470 ohm

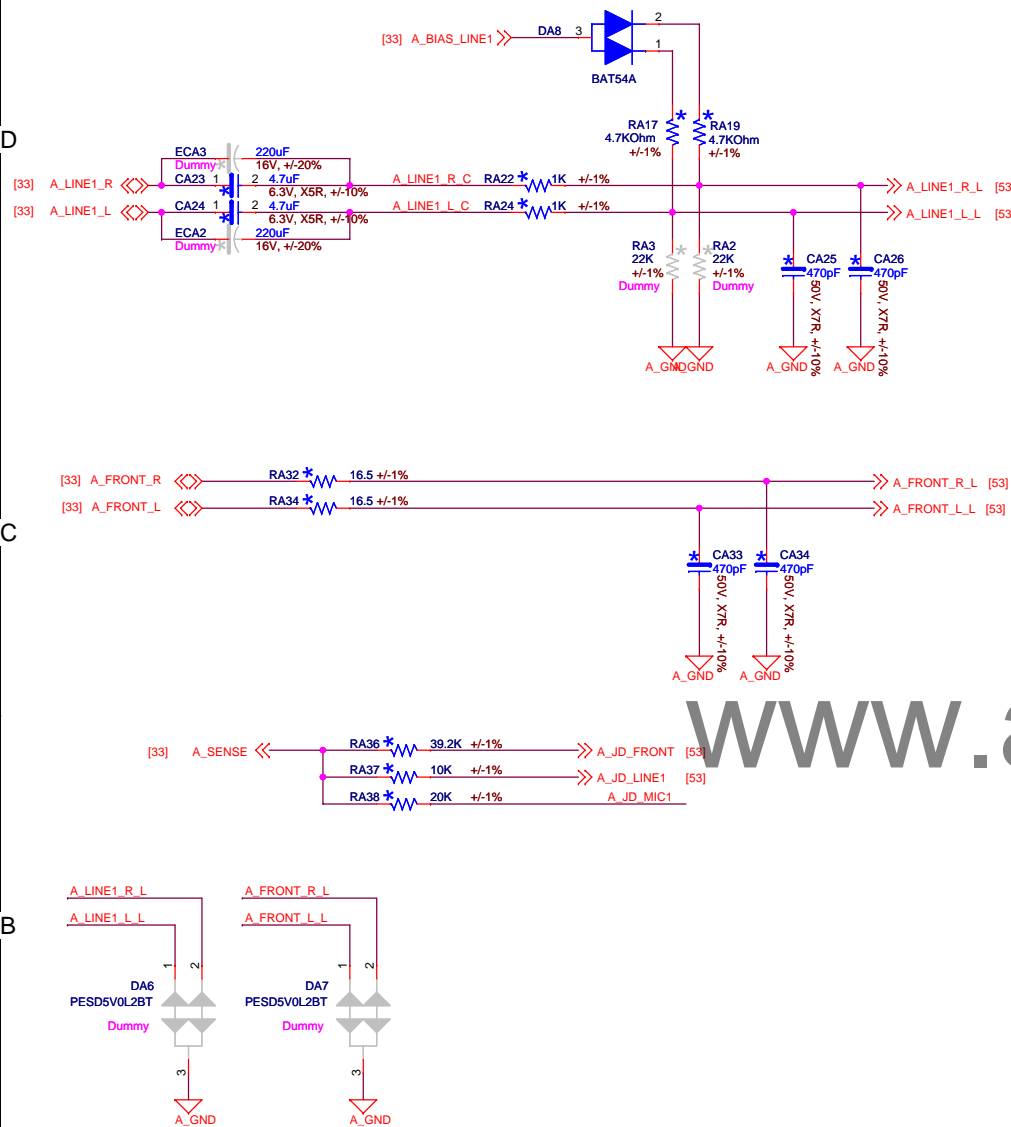


LAN POWER



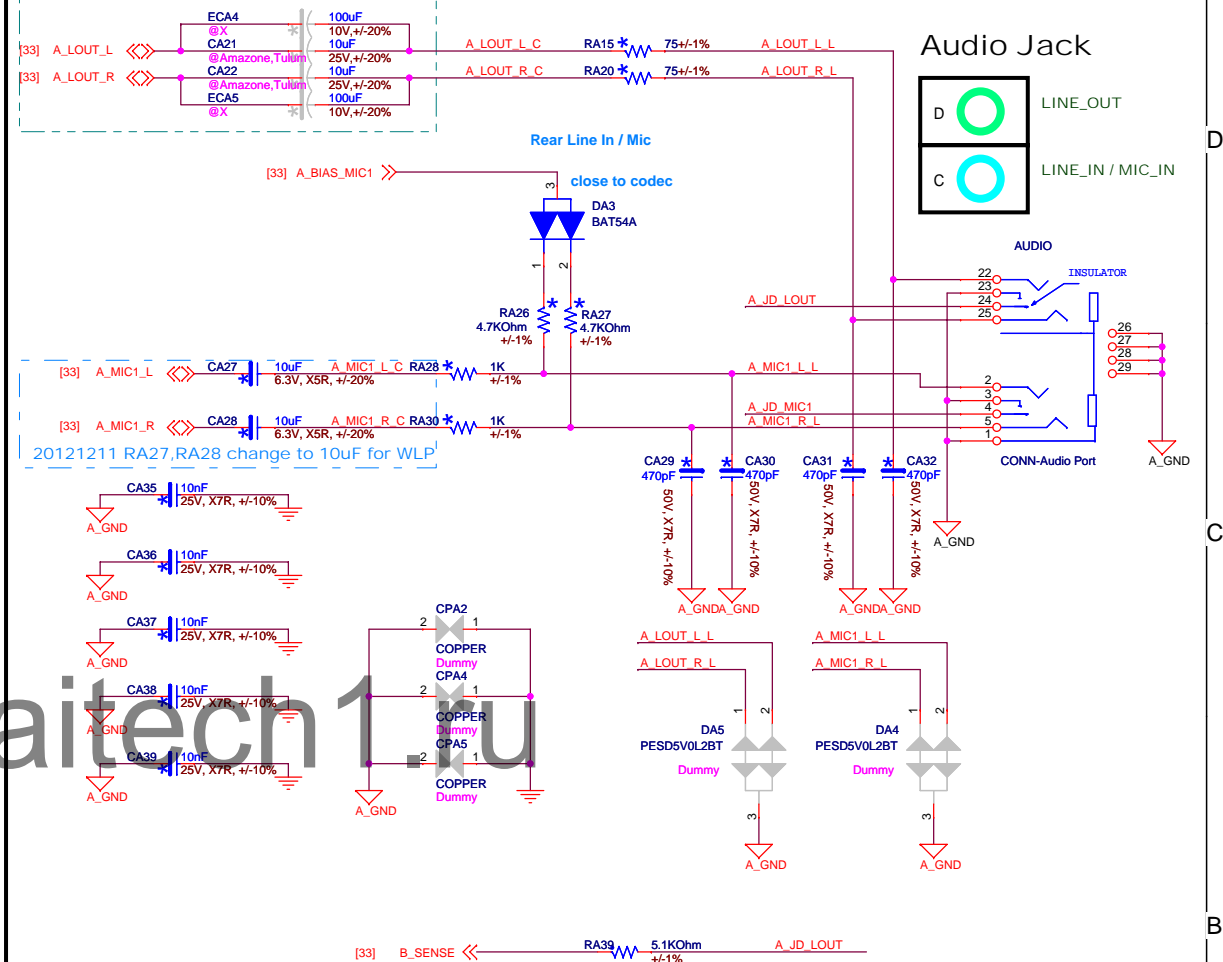


Front Audio



Rear Audio Jack

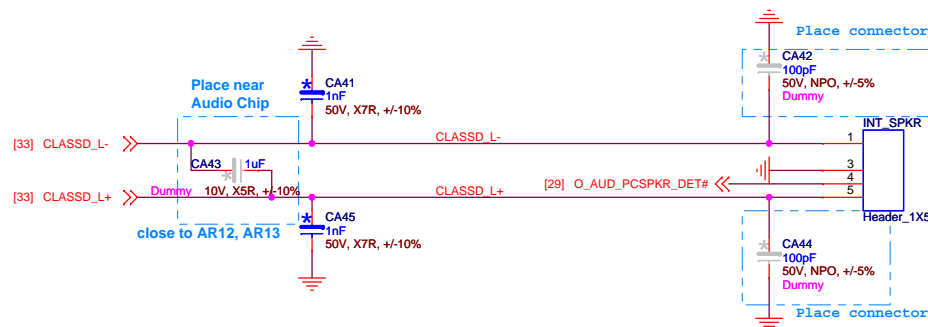
20120626: Add ECA4 co-lay with CA21 : ECA5 co-lay with CA22
20120829: ECA4, ECA5 change to 100uF and CA21, CA22 add remark option



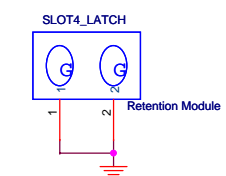
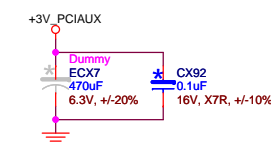
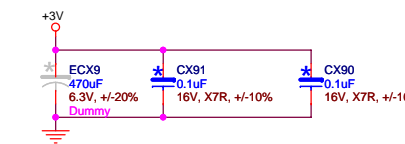
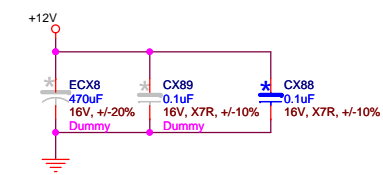
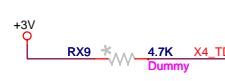
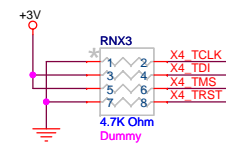
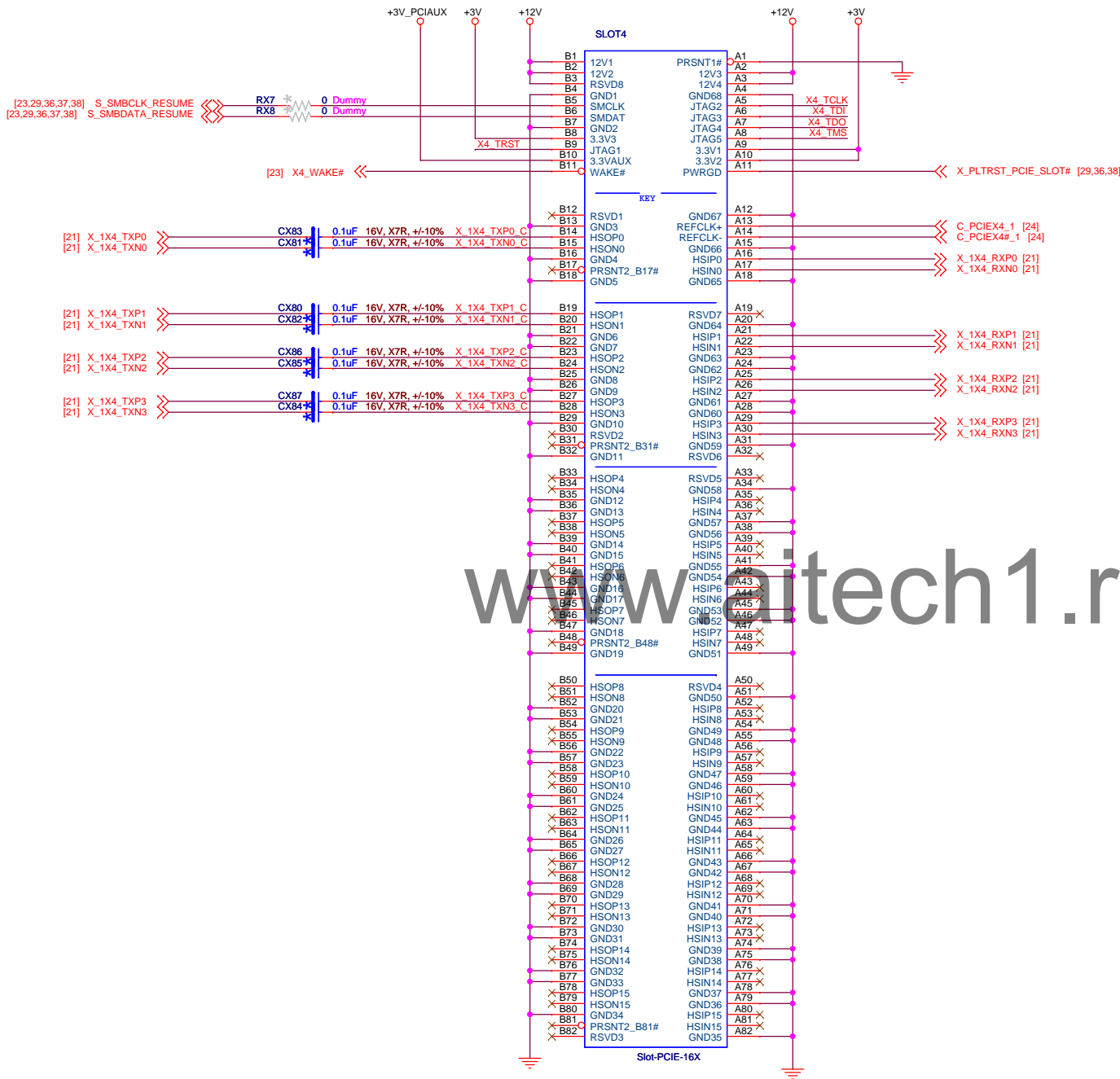
CHASSIS SPEAKER

Header 1x5 cut2

Pin.1--> Left-
Pin.2--> NC key
Pin.3--> GND
Pin.4--> SPK det#
Pin.5--> Left+



| | | |
|------------|---------------------------|----------------|
| Title | | |
| Audio Conn | | |
| DWG NO | Tulum/Amazon MT | Rev A00 |
| Date | Tuesday, January 29, 2013 | Sheet 34 of 66 |



www.nitech1.ru

| | | | |
|--------|---------------------------|---------|----------|
| | | Title | |
| | | PCIe 4x | |
| DWG NO | Tulum/Amazon MT | | Rev |
| | | | A00 |
| Date: | Tuesday, January 29, 2013 | Sheet | 35 of 66 |

[12] X_1X16_TXP[15..0]
[12] X_1X16_TXN[15..0]

[23,29,35,37,38] S_SMBCLK_RESUME
[23,29,35,37,38] S_SMBDATA_RESUME

[20,23,55] S_WAKE#

X_1X16_TXP0 CX45 220nF 16V X7R +/-10% X EXP A TX C DP0
X_1X16_TXN0 CX47 220nF 16V X7R +/-10% X EXP A TX C DN0

X_1X16_TXP1 CX66 220nF 16V X7R +/-10% X EXP A TX C DP1
X_1X16_TXN1 CX73 220nF 16V X7R +/-10% X EXP A TX C DN1

X_1X16_TXP2 CX44 220nF 16V X7R +/-10% X EXP A TX C DP2
X_1X16_TXN2 CX53 220nF 16V X7R +/-10% X EXP A TX C DN2

X_1X16_TXP3 CX63 220nF 16V X7R +/-10% X EXP A TX C DP3
X_1X16_TXN3 CX72 220nF 16V X7R +/-10% X EXP A TX C DN3

X_1X16_TXP4 CX78 220nF 16V X7R +/-10% X EXP A TX C DP4
X_1X16_TXN4 CX49 220nF 16V X7R +/-10% X EXP A TX C DN4

X_1X16_TXP5 CX50 220nF 16V X7R +/-10% X EXP A TX C DP5
X_1X16_TXN5 CX64 220nF 16V X7R +/-10% X EXP A TX C DN5

X_1X16_TXP6 CX71 220nF 16V X7R +/-10% X EXP A TX C DP6
X_1X16_TXN6 CX79 220nF 16V X7R +/-10% X EXP A TX C DN6

X_1X16_TXP7 CX47 220nF 16V X7R +/-10% X EXP A TX C DP7
X_1X16_TXN7 CX54 220nF 16V X7R +/-10% X EXP A TX C DN7

X_1X16_TXP8 CX52 220nF 16V X7R +/-10% X EXP A TX C DP8
X_1X16_TXN8 CX65 220nF 16V X7R +/-10% X EXP A TX C DN8

X_1X16_TXP9 CX82 220nF 16V X7R +/-10% X EXP A TX C DP9
X_1X16_TXN9 CX70 220nF 16V X7R +/-10% X EXP A TX C DN9

X_1X16_TXP10 CX69 220nF 16V X7R +/-10% X EXP A TX C DP10
X_1X16_TXN10 CX76 220nF 16V X7R +/-10% X EXP A TX C DN10

X_1X16_TXP11 CX68 220nF 16V X7R +/-10% X EXP A TX C DP11
X_1X16_TXN11 CX75 220nF 16V X7R +/-10% X EXP A TX C DN11

X_1X16_TXP12 CX74 220nF 16V X7R +/-10% X EXP A TX C DP12
X_1X16_TXN12 CX46 220nF 16V X7R +/-10% X EXP A TX C DN12

X_1X16_TXP13 CX43 220nF 16V X7R +/-10% X EXP A TX C DP13
X_1X16_TXN13 CX51 220nF 16V X7R +/-10% X EXP A TX C DN13

X_1X16_TXP14 CX77 220nF 16V X7R +/-10% X EXP A TX C DP14
X_1X16_TXN14 CX48 220nF 16V X7R +/-10% X EXP A TX C DN14

X_1X16_TXP15 CX56 220nF 16V X7R +/-10% X EXP A TX C DP15
X_1X16_TXN15 CX55 220nF 16V X7R +/-10% X EXP A TX C DN15

SLOT1

B1 12V1
B2 12V2
B3 RSVDB
B4 GND1
B5 GND1
B6 GND1
B7 SMDAT
B8 GND2
B9 JTAG3
B10 JTAG5
B11 3.3V1
B12 3.3V2
B13 WAKE#
B14 PRSNT2_B17#
B15 GND5

B12 RSVDB
B13 GND3
B14 HSON0
B15 HSON0
B16 HSON0
B17 PRSNT2_B17#
B18 GND5

B19 HSON1
B20 GND6
B21 GND6
B22 GND7
B23 HSON2
B24 GND8
B25 HSON2
B26 GND8
B27 HSON3
B28 GND9
B29 HSON3
B30 GND10
B31 PRSNT2_B31#
B32 GND11

B33 HSON4
B34 GND12
B35 HSON4
B36 GND13
B37 HSON5
B38 GND14
B39 HSON5
B40 GND15
B41 HSON6
B42 GND16
B43 HSON6
B44 GND17
B45 HSON7
B46 GND18
B47 PRSNT2_B48#
B48 GND19

B50 HSON8
B51 GND20
B52 GND20
B53 GND21
B54 HSON9
B55 GND22
B56 HSON9
B57 GND23
B58 HSON10
B59 GND24
B60 HSON10
B61 GND25
B62 HSON11
B63 GND26
B64 HSON11
B65 GND27
B66 HSON12
B67 GND28
B68 HSON12
B69 GND29
B70 HSON13
B71 GND30
B72 HSON13
B73 GND31
B74 HSON14
B75 GND32
B76 HSON14
B77 GND33
B78 HSON15
B79 GND34
B80 HSON15
B81 PRSNT2_B81#
B82 RSVDB

Slot-PCIE-16X

Used PCH GPIO13 PCIE RESET Mode:
Stuffed => RX11
Dummy => RX10

RX10 0 Dummy
RX11 0 X_RST_SLOT_PEG# X_PLTRST_PCIE_SLOT# [29,35,38]

C_PCIE16_1 [24]
C_PCIE16#_1 [24]

X_1X16_RXP0
X_1X16_RXN0

X_1X16_RXP1
X_1X16_RXN1

X_1X16_RXP2
X_1X16_RXN2

X_1X16_RXP3
X_1X16_RXN3

X_1X16_RXP4
X_1X16_RXN4

X_1X16_RXP5
X_1X16_RXN5

X_1X16_RXP6
X_1X16_RXN6

X_1X16_RXP7
X_1X16_RXN7

X_1X16_RXP8
X_1X16_RXN8

X_1X16_RXP9
X_1X16_RXN9

X_1X16_RXP10
X_1X16_RXN10

X_1X16_RXP11
X_1X16_RXN11

X_1X16_RXP12
X_1X16_RXN12

X_1X16_RXP13
X_1X16_RXN13

X_1X16_RXP14
X_1X16_RXN14

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

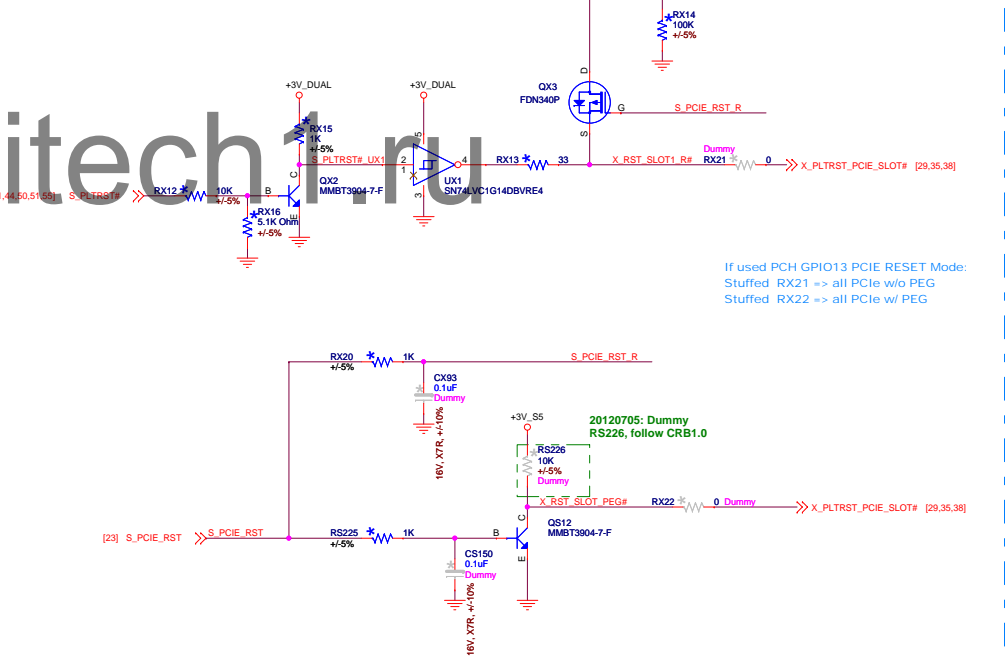
X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

X_1X16_RXP15
X_1X16_RXN15

PCIE RESET LOGIC CIRCUIT

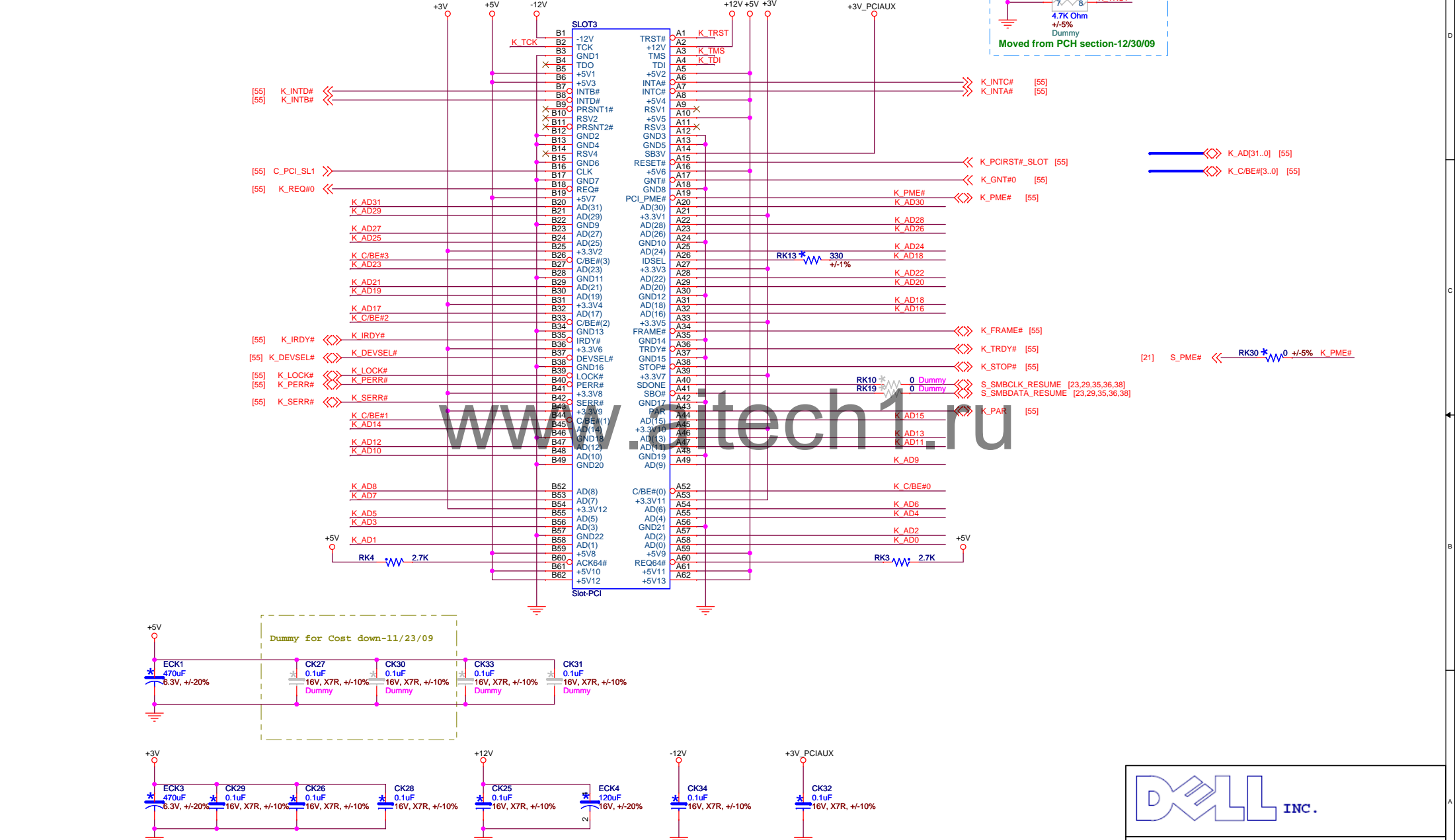
Used PCH GPIO13 PCIE RESET Mode:
Stuffed => RX12, RX20, RS225

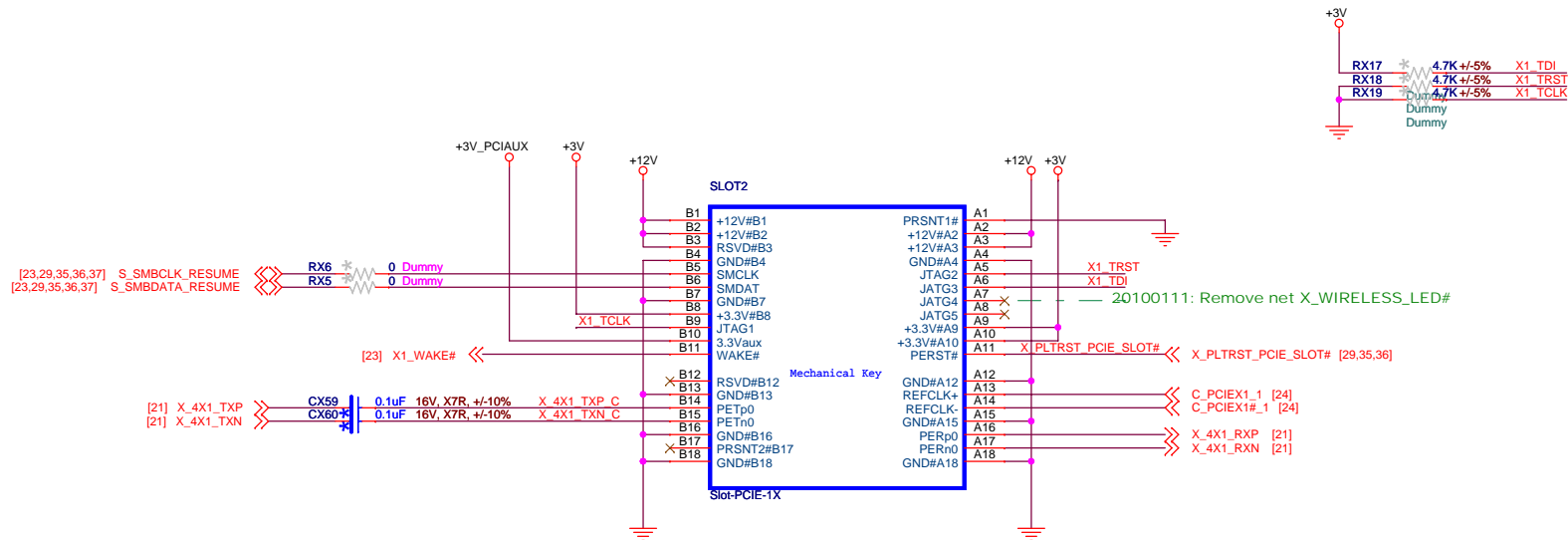


If used PCH GPIO13 PCIE RESET Mode:
Stuffed RX21 => all PCIe w/o PEG
Stuffed RX22 => all PCIe w/ PEG

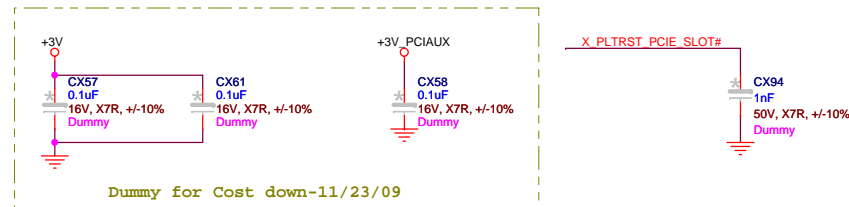


IRQ: CDAB
IDSEL: AD18
REQ/GNT: 0



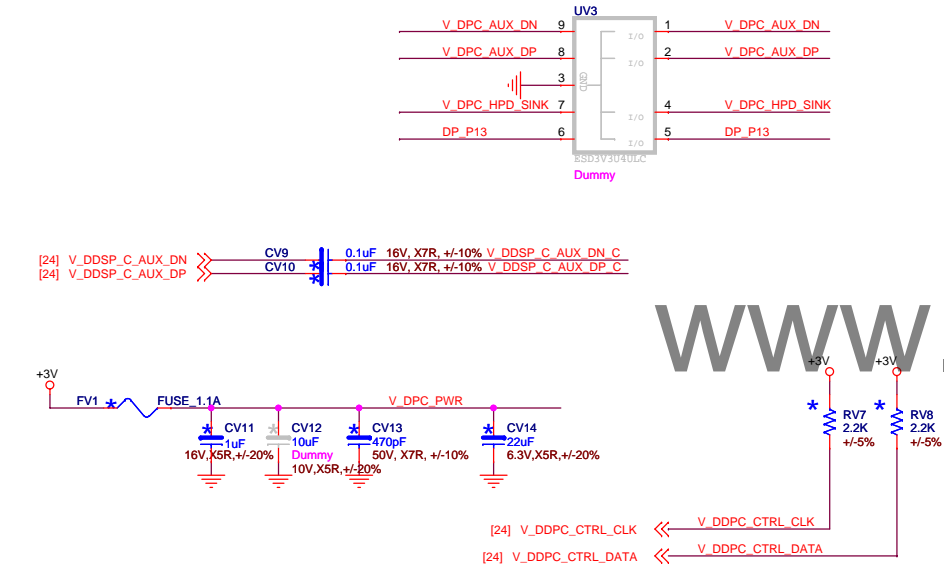
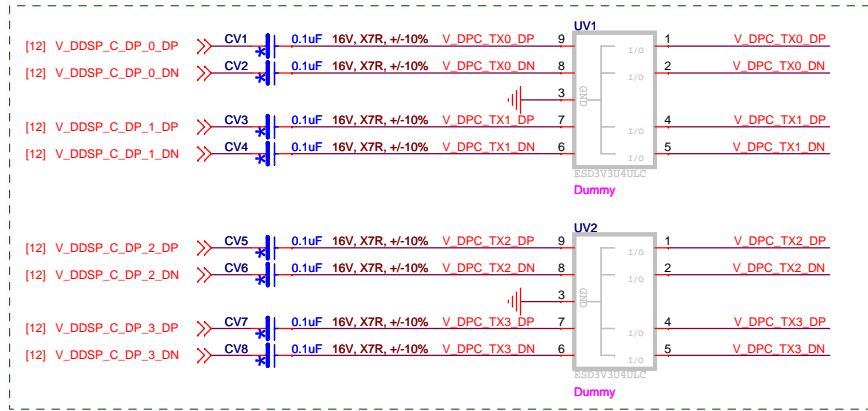


www.aitech1.ru



| | |
|---------------------------------|----------------|
| | |
| | |
| Title | |
| PCIe 1x | |
| DWG NO | Rev |
| Tulum/Amazon MT | A00 |
| Date: Tuesday, January 29, 2013 | Sheet 38 of 66 |

20120521: Delete UV4 ; UV1, UV2, UV3 change to INFINEON_ESD3V3U4ULC



20120521: Delete UV8 : UV7, UV9, UV10 change to INFINEON_ESD3V3U4ULC

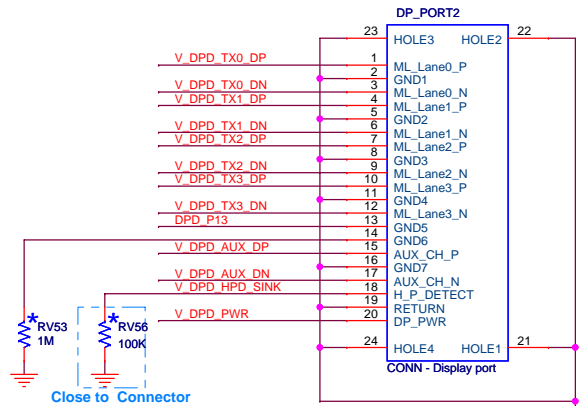
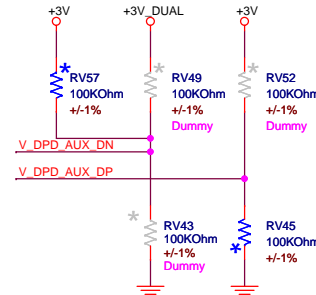
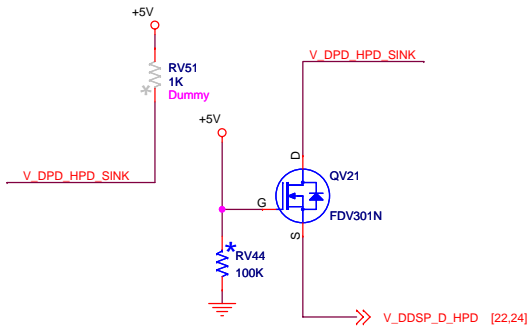
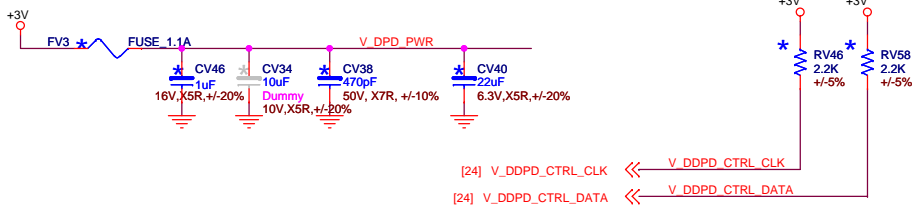
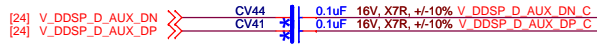
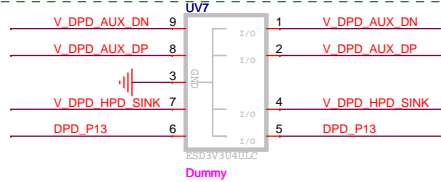
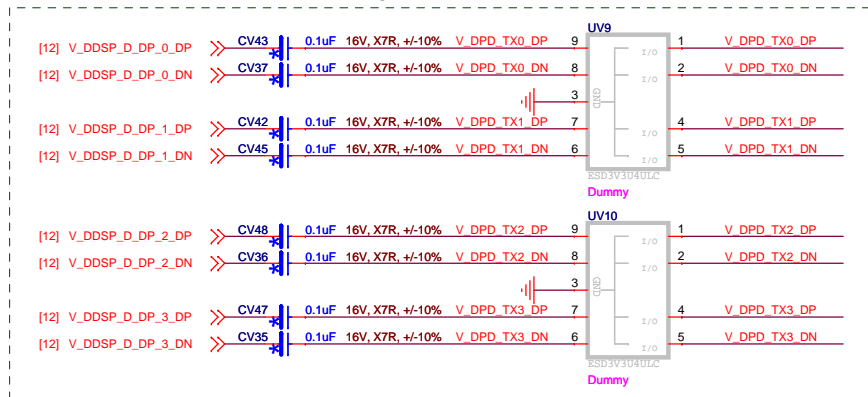
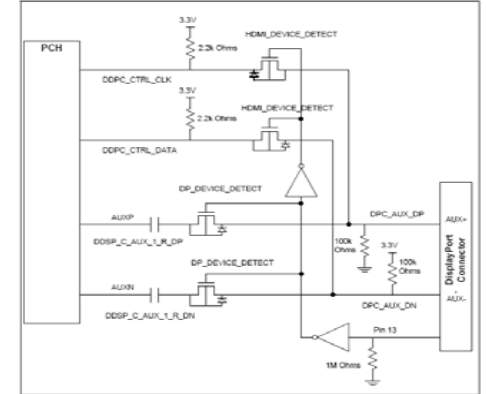
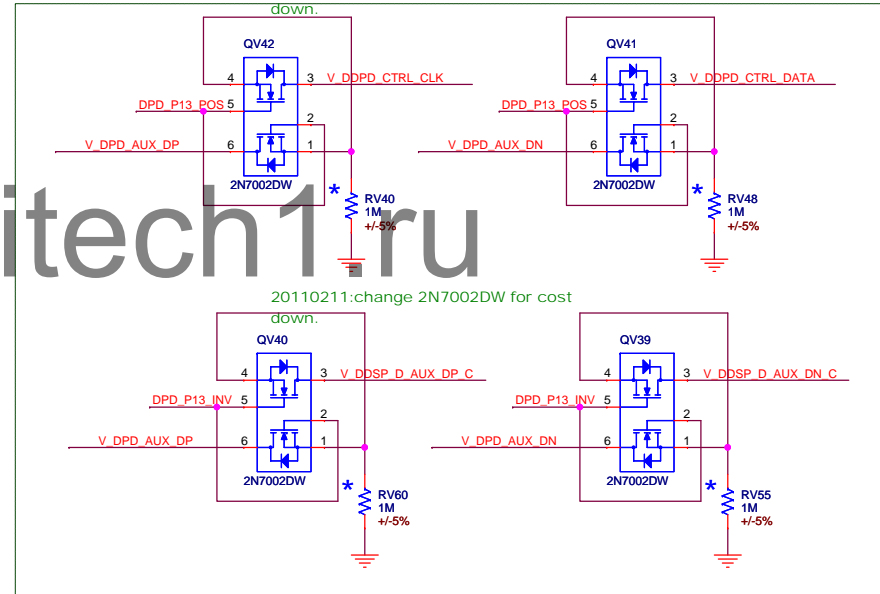


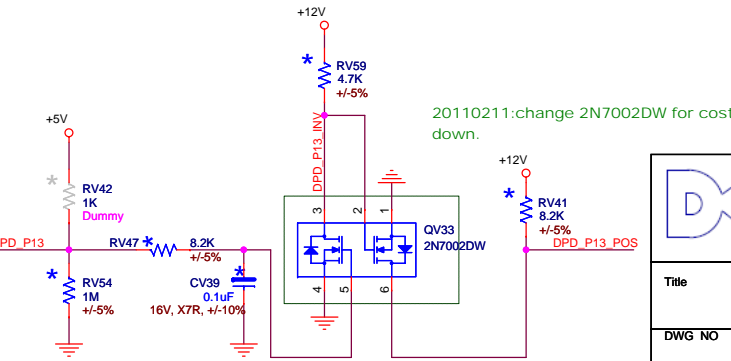
Figure 7-5. DisplayPort Interoperability Implementation



20110211:change 2N7002DW for cost down.



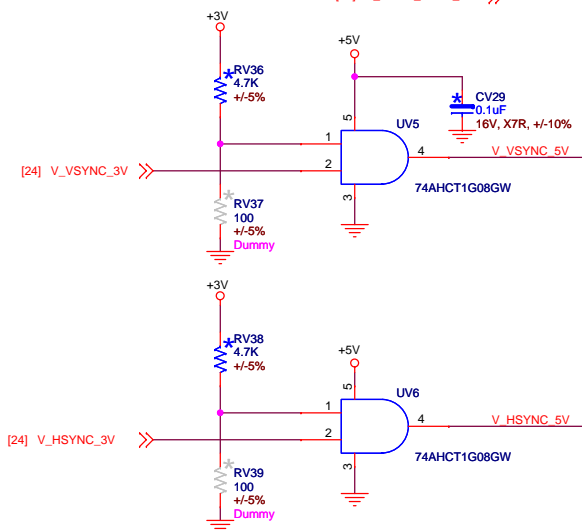
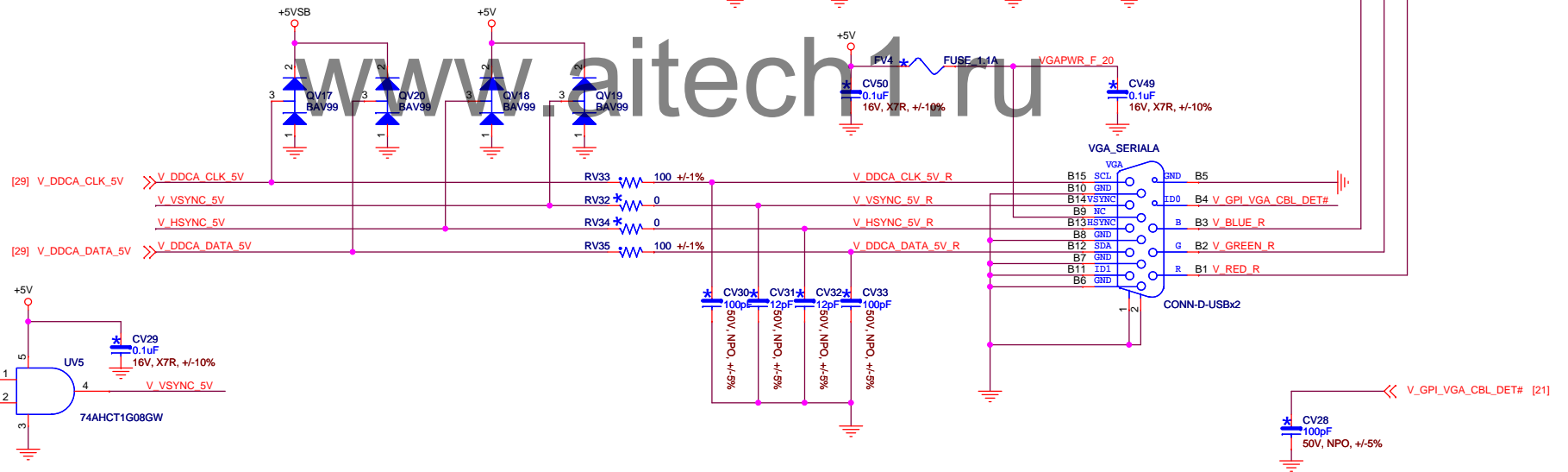
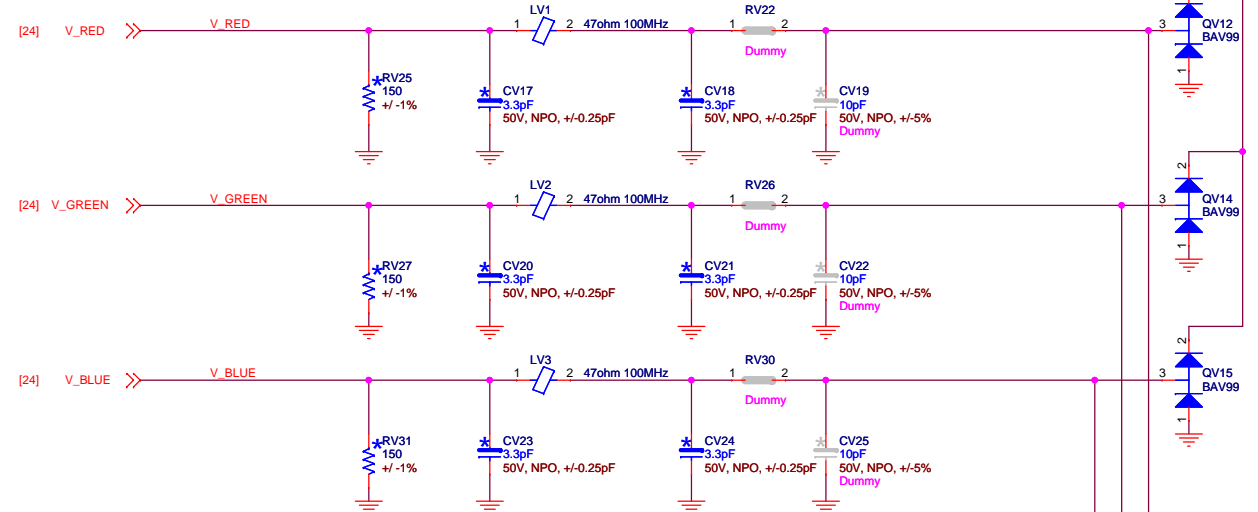
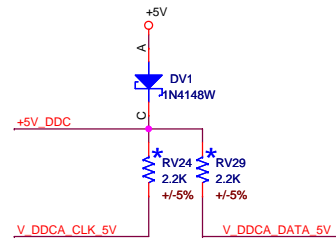
20110211:change 2N7002DW for cost down.



20110211:change 2N7002DW for cost down.

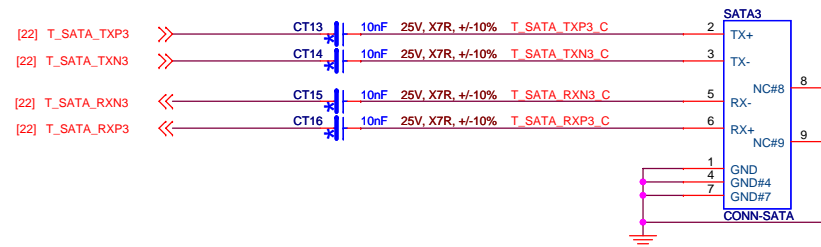
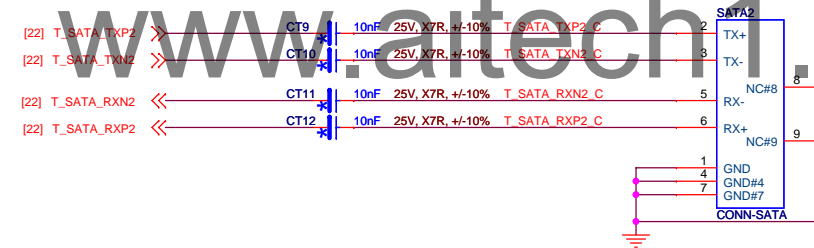
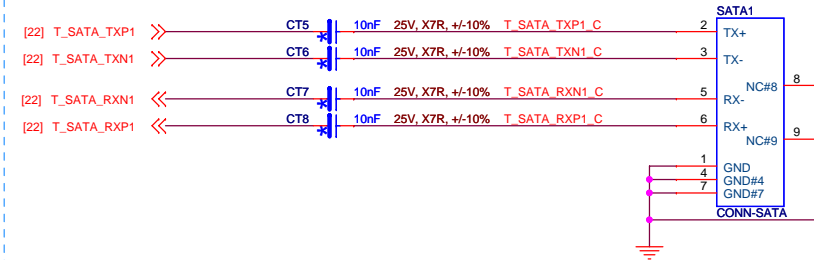
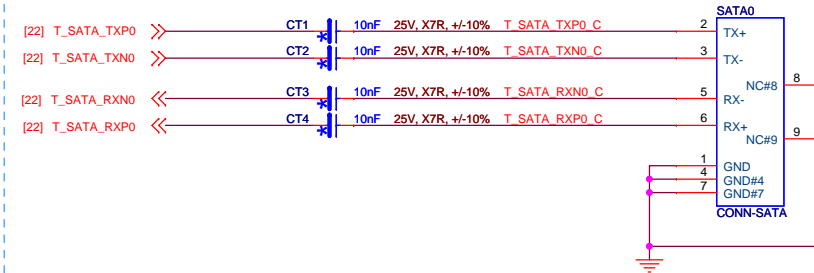
| | | |
|--------------------------|---|-----------------------|
| | | |
| Display Port 2 | | |
| Title DWG NO Date: | Tulum/Amazon MT Rev Tuesday, January 29, 2013 | A00 Sheet 40 of 66 |

VGA Connector

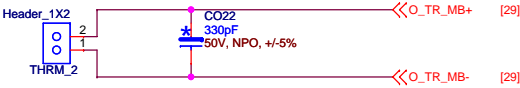


| | | | |
|------------------------|---------------------------|------------|----------|
| Title | | | |
| VGA Conn | | | |
| DWG NO | | Rev | |
| <i>Tulum/Amazon MT</i> | | A00 | |
| Date: | Tuesday, January 29, 2013 | Sheet | 41 of 66 |

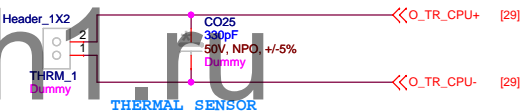
SATA Gen.3



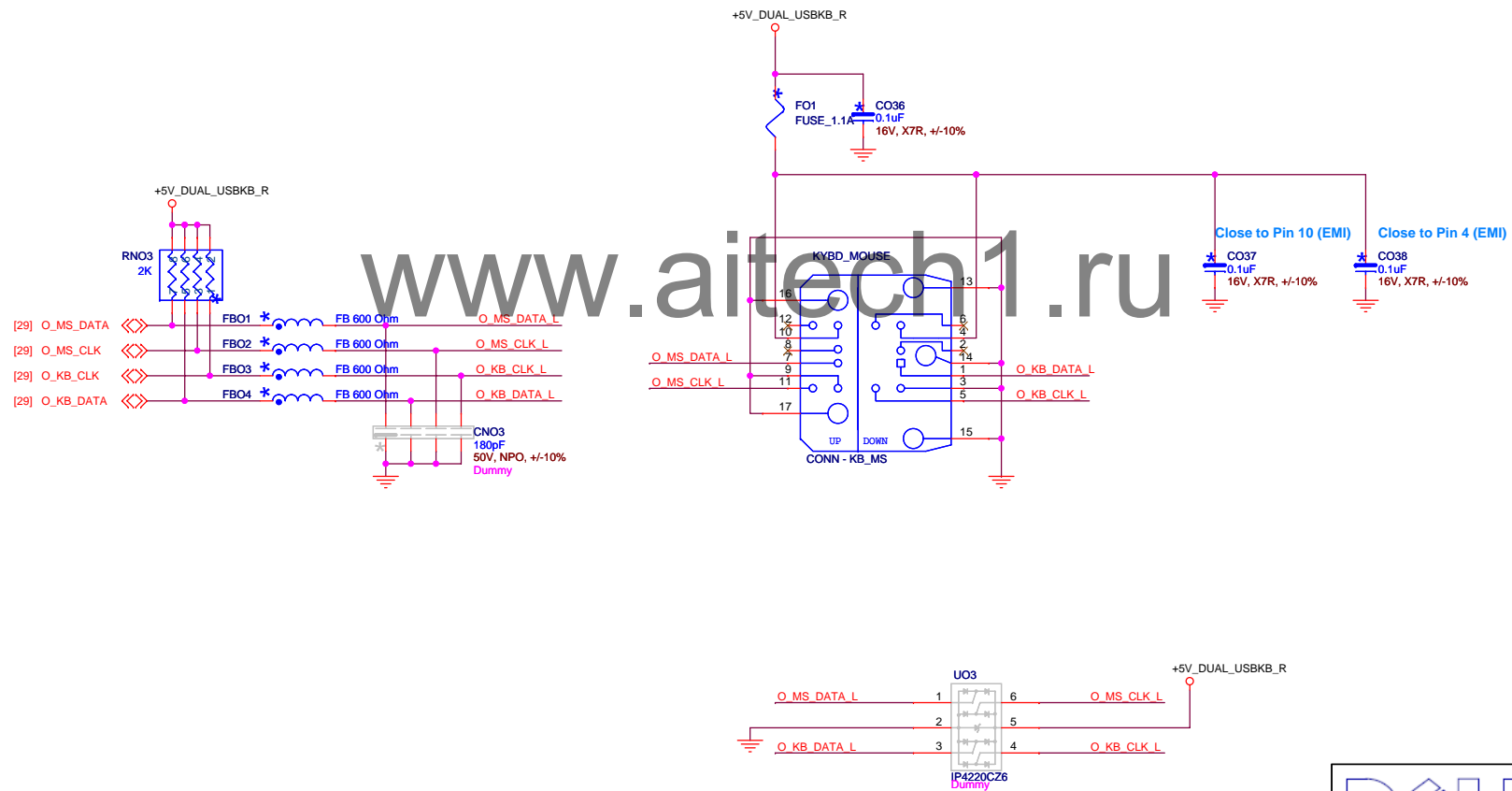
| | | |
|---------------------------------|-----------------|---------|
| Title | | |
| SATA Conn | | |
| DWG NO | Tulum/Amazon MT | Rev A00 |
| Date: Tuesday, January 29, 2013 | Sheet 42 of 66 | |



Dummy THRM2,CO23; ME suggestion-12/04/09



KB/MS



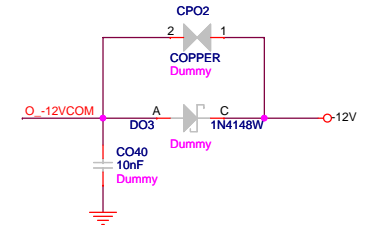
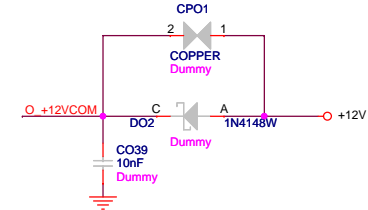
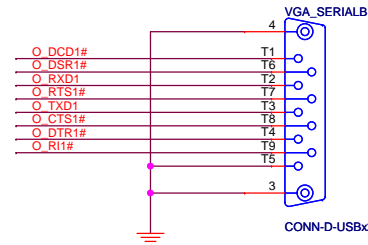
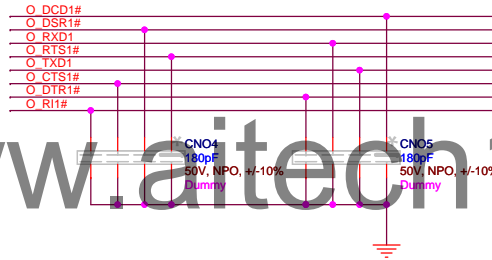
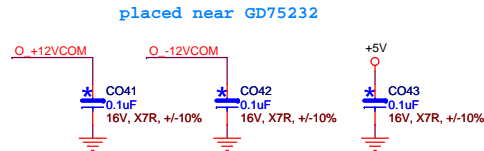
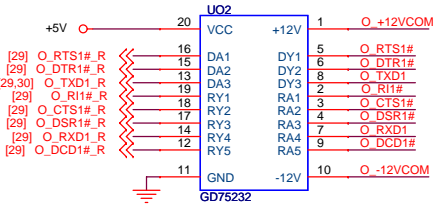
DELL INC.

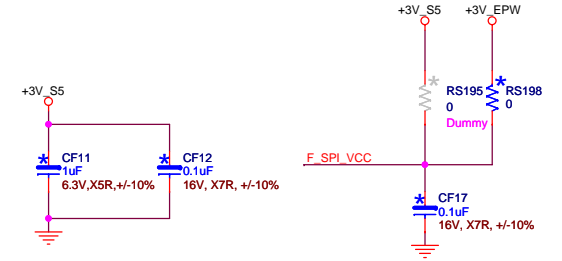
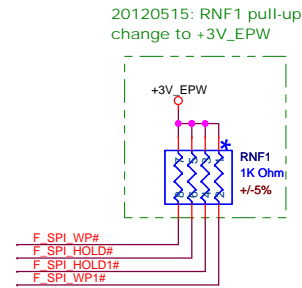
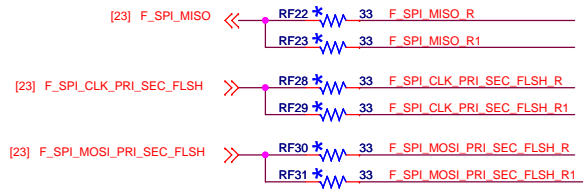
Title: **PS2 Conn**

DWG NO: **Tulum/Amazon MT** Rev: **A00**

Date: Tuesday, January 29, 2013 Sheet 47 of 66

Serial Port 1

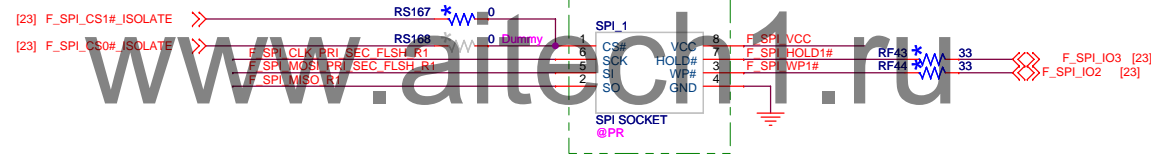
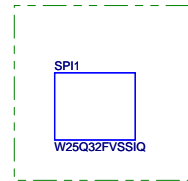




SPI_4MB

20110530: SPI1 Change to 4M

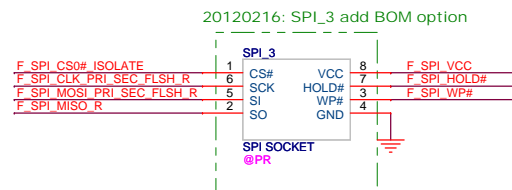
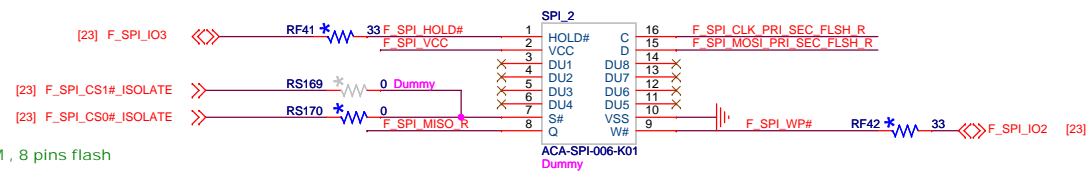
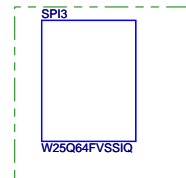
20120216: SPI1 Change to WINBOND_W25Q32BVSSIG



SPI_8MB

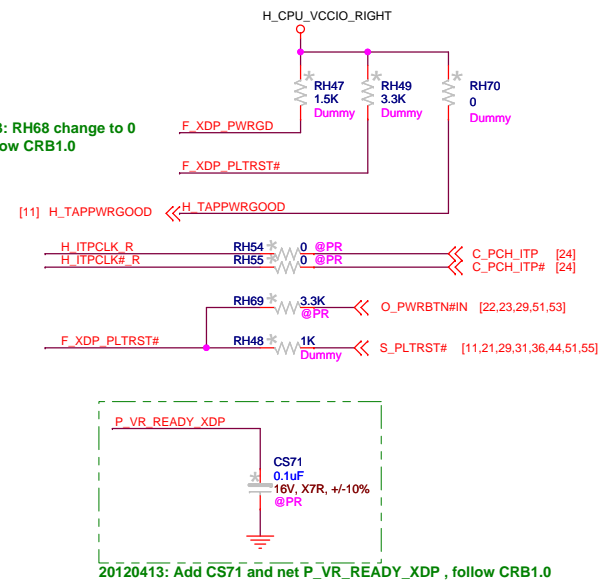
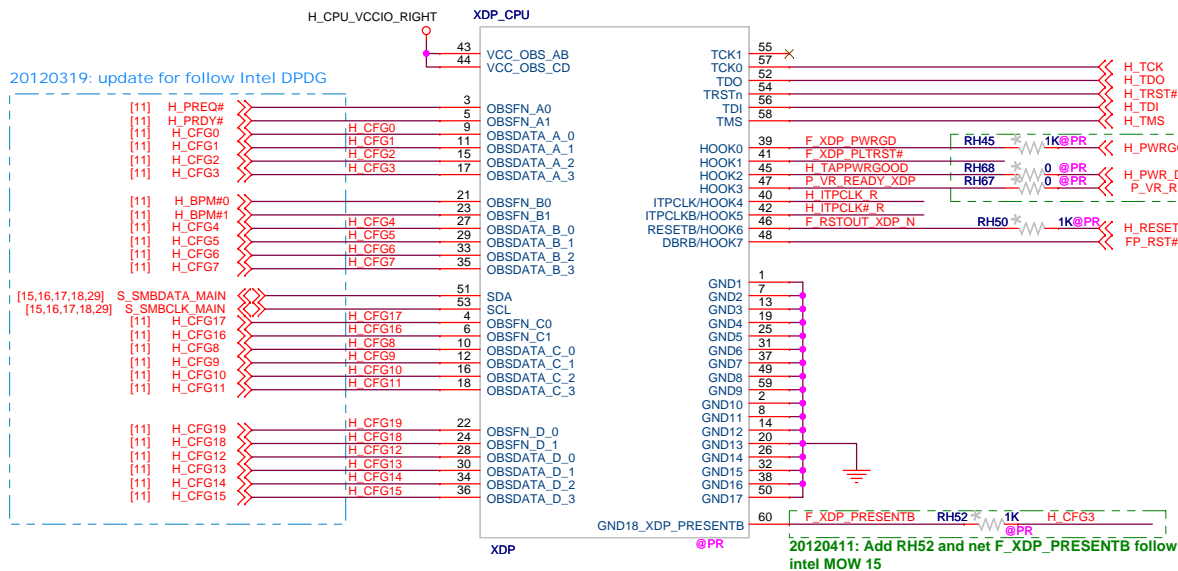
20120216: SPI2 rename to SPI3 and Change to 8M , 8 pins flash

20120216: SPI3 and Change to 8M , 8 pins flash, WINBOND_W25Q64FVSSIG

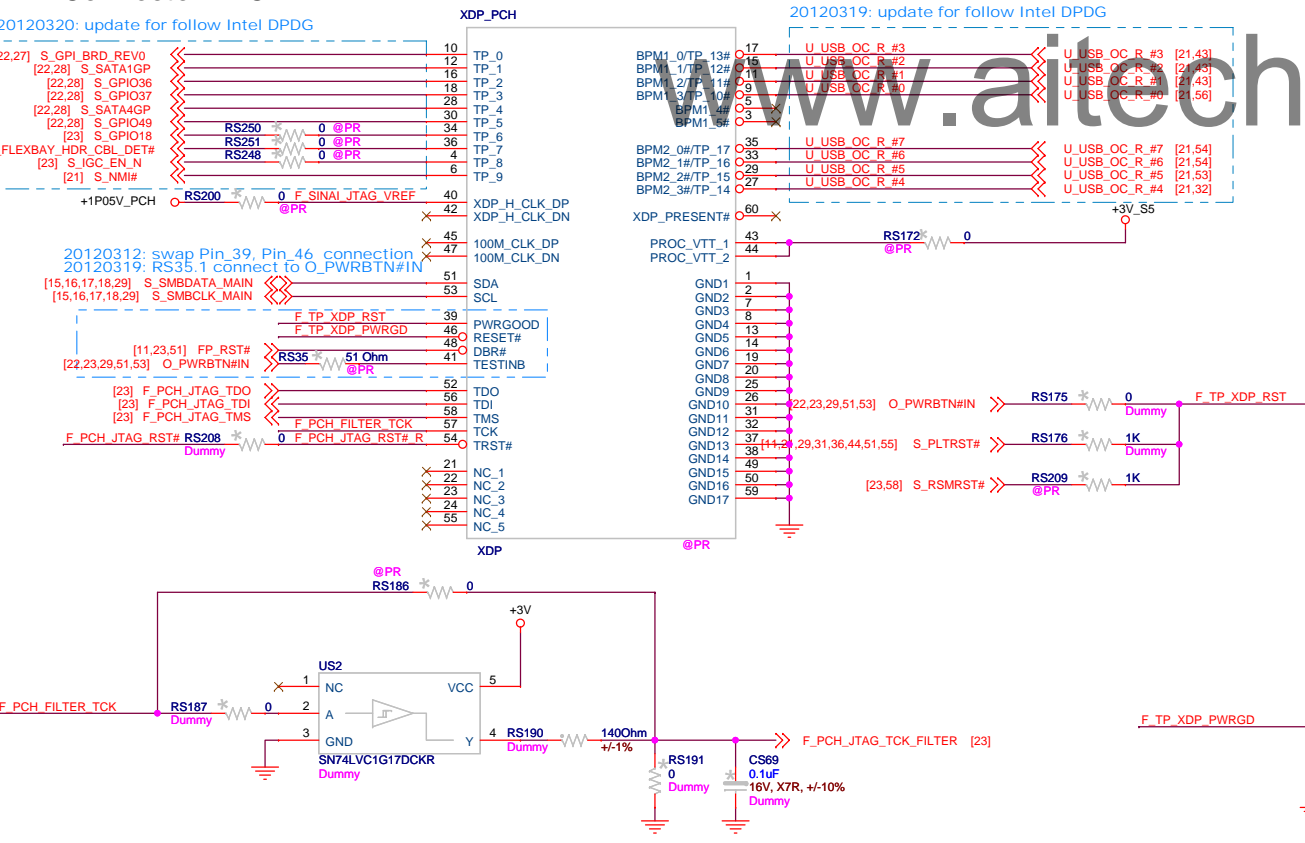


| | |
|---------------------------------|----------------|
| | |
| | |
| Title | |
| SPI | |
| DWG NO | Rev |
| Tulum/Amazon MT | A00 |
| Date: Tuesday, January 29, 2013 | Sheet 49 of 66 |

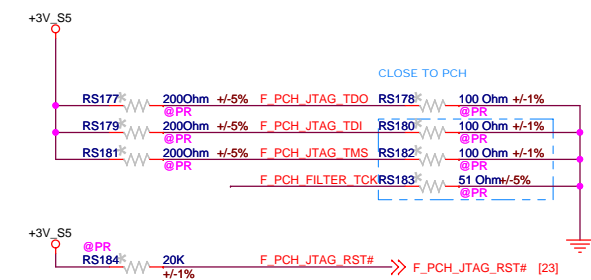
XDP Connector - CPU



XDP Connector - PCH

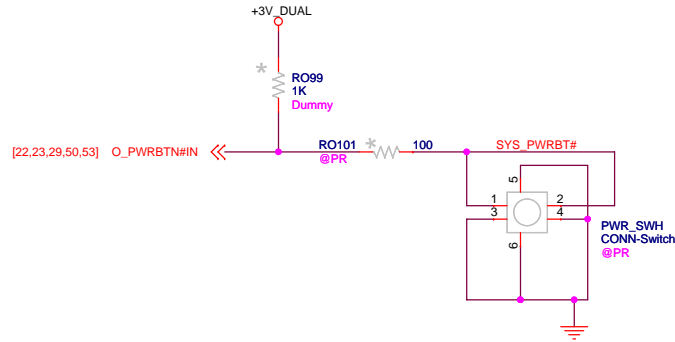


| 2009/12/21 Update JTAG Table | | PCH JTAG Enable | | PCH JTAG Disable | |
|------------------------------|-------|-----------------|-----------------------|------------------|----------|
| | | ES1 | ES2 | ES1 | ES2 |
| F_PCH_JTAG_TDO | RS177 | No Stff | 200 Ohms ¹ | No Stuff | No Stuff |
| | RS178 | No Stff | 100 Ohms ¹ | No Stuff | No Stuff |
| F_PCH_JTAG_TMS | RS179 | 200 Ohms | 200 Ohms | No Stuff | No Stuff |
| | RS180 | 100 Ohms | 100 Ohms | No Stuff | No Stuff |
| F_PCH_JTAG_TDI | RS181 | 200 Ohms | 200 Ohms | 20K Ohms | No Stuff |
| | RS182 | 100 Ohms | 100 Ohms | 10K Ohms | No Stuff |
| F_PCH_FILTER_TCK | RS183 | 51 Ohms | 51 Ohms | 51 Ohms | 51 Ohms |
| F_PCH_JTAG_RST# | RS184 | 20K Ohms | 20K Ohms | No Stuff | No Stuff |
| | RS185 | 10K Ohms | 10K Ohms | No Stuff | No Stuff |

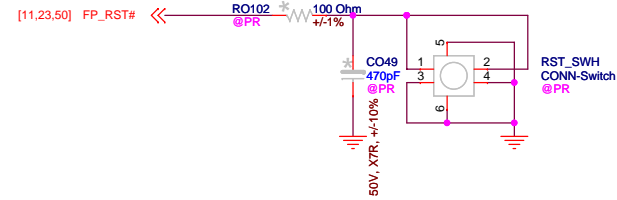


| | | | |
|------------------------|---------------------------|-------|------------|
| Title | | | |
| XDP | | | |
| DWG NO | | | Rev |
| <i>Tulum/Amazon MT</i> | | | A00 |
| Date: | Tuesday, January 29, 2013 | Sheet | 50 of 66 |

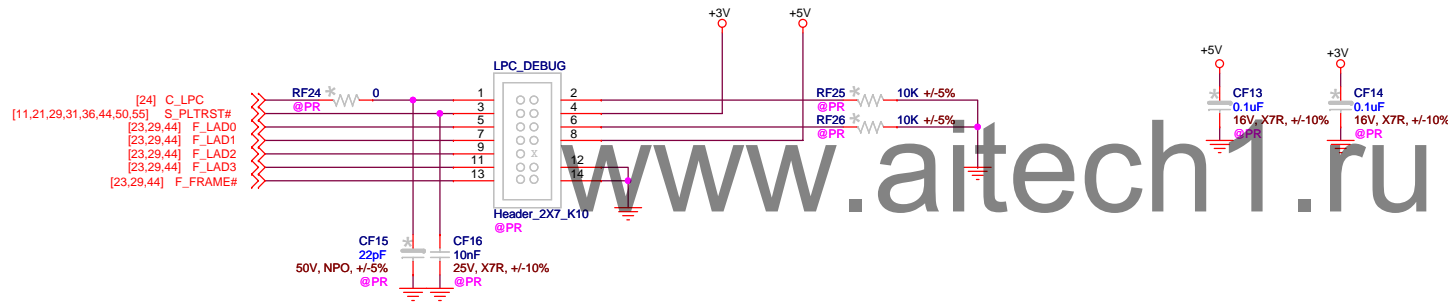
Power Bottom



Reset Bottom

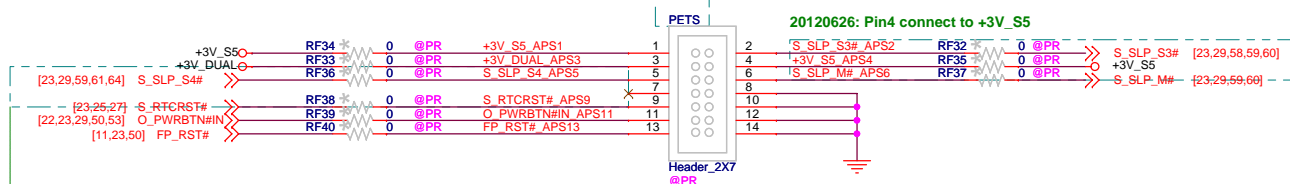


LPC DEBUG



APS Debug

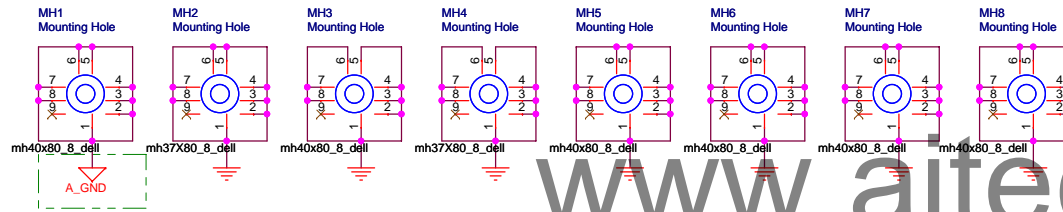
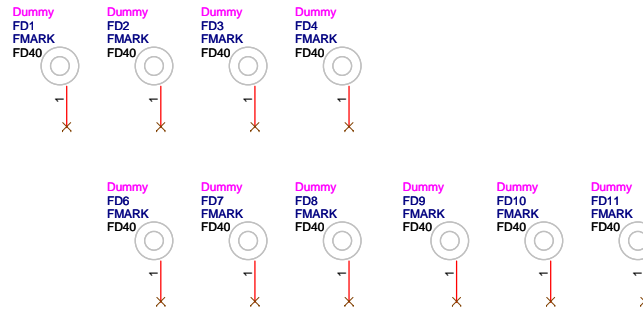
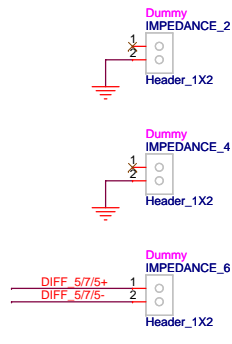
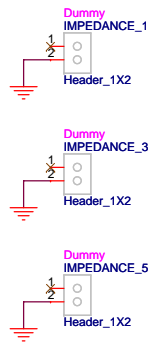
20120621: rename to PETS



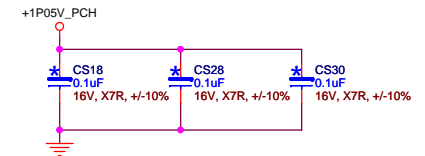
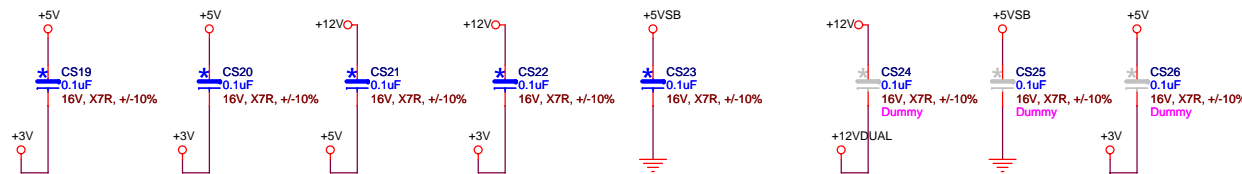
20120626: Pin7 net rename to +3V_DUAL_APS7 and add RF49 connect to +3V_DUAL
20120626: Pin7 let NC

| Desktop | | |
|---------------|------------|---|
| APS Connector | Pin | Meaning |
| Pin 1 | VccSus3_3 | 3.3 V Suspend Power Well |
| Pin 2 | SLP_S3# | When asserted (0) system is in S3 |
| Pin 3 | VccDSW3_3 | Used to determine if system is in Deep Sx |
| Pin 4 | VccSus3_3 | When off (0) system is in S5 |
| Pin 5 | SLP_S4# | When asserted (0) system is in S4 |
| Pin 6 | SLP_A# | When asserted (0) ME is in Moff |
| Pin 7 | | Unused |
| Pin 8 | GND | Ground |
| Pin 9 | RTCST# | When asserted (0) CMOS is cleared |
| Pin 10 | GND | Ground for RTCST# |
| Pin 11 | PWRBTN# | When asserted (0) Power Button Pushed |
| Pin 12 | GND | Ground for PWRBTN# |
| Pin 13 | SYS_RESET# | When asserted (0) Reset Button Pushed |
| Pin 14 | GND | Ground for SYS_RESET# |

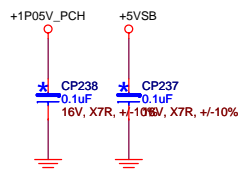




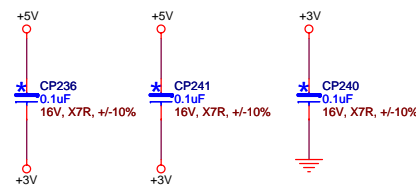
www.aitech1.ru



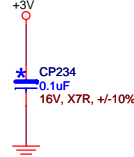
for H_ITPCLK.



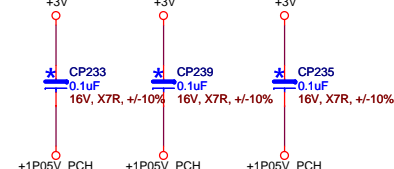
for C_PCI_SB.



for A_Z_Bitclk.



for Front USB3.0



| | | |
|---------------------------------|-----------------|---------|
| | | |
| | | |
| Title | | |
| EMI | | |
| DWG NO | Tulum/Amazon MT | Rev A00 |
| Date: Tuesday, January 29, 2013 | Sheet 52 of 66 | |

Front USB/LED Header

20120214: USB3_FRONT connector change to PUB200-2017-B5-10-HF.

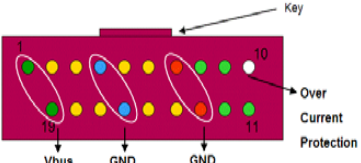
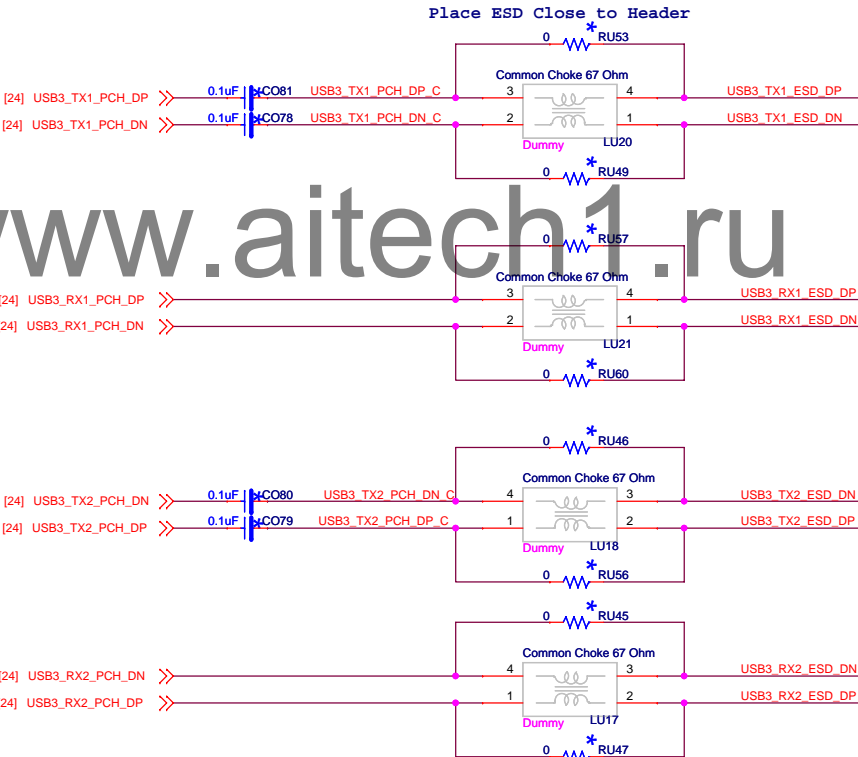
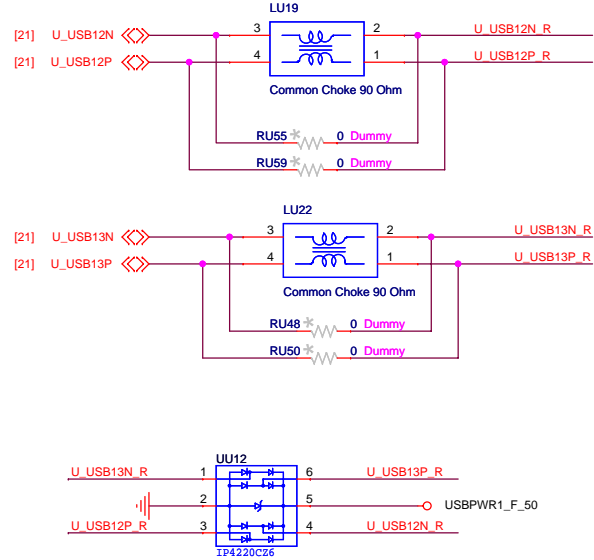
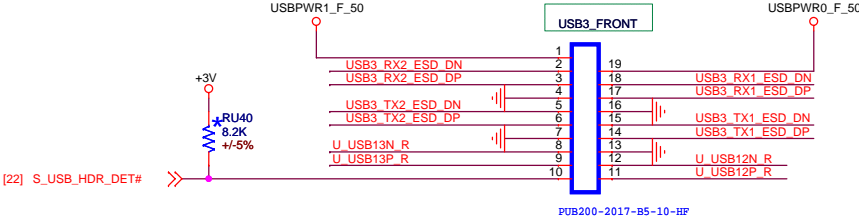
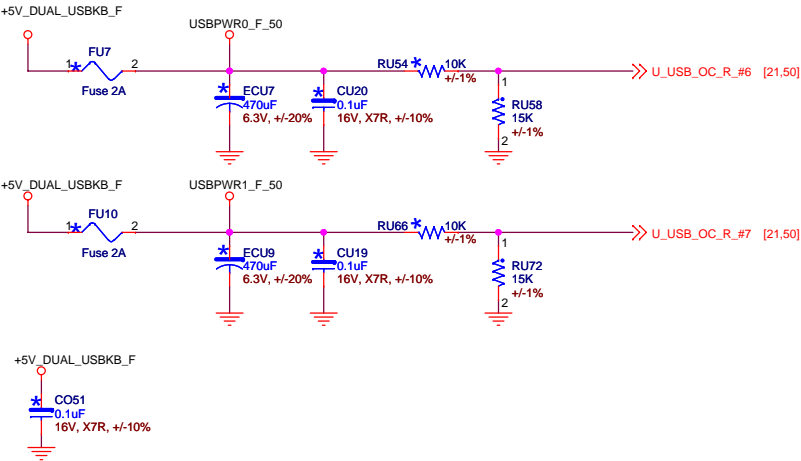
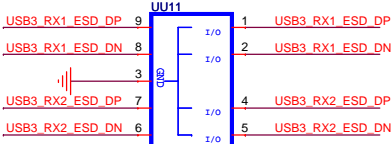
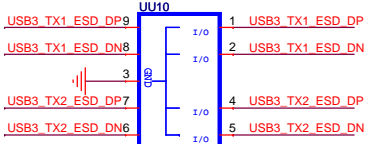
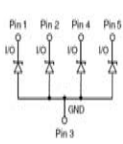
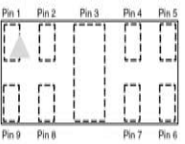
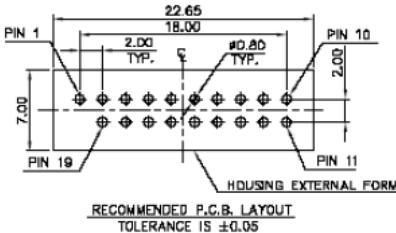
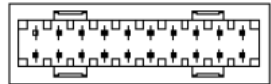
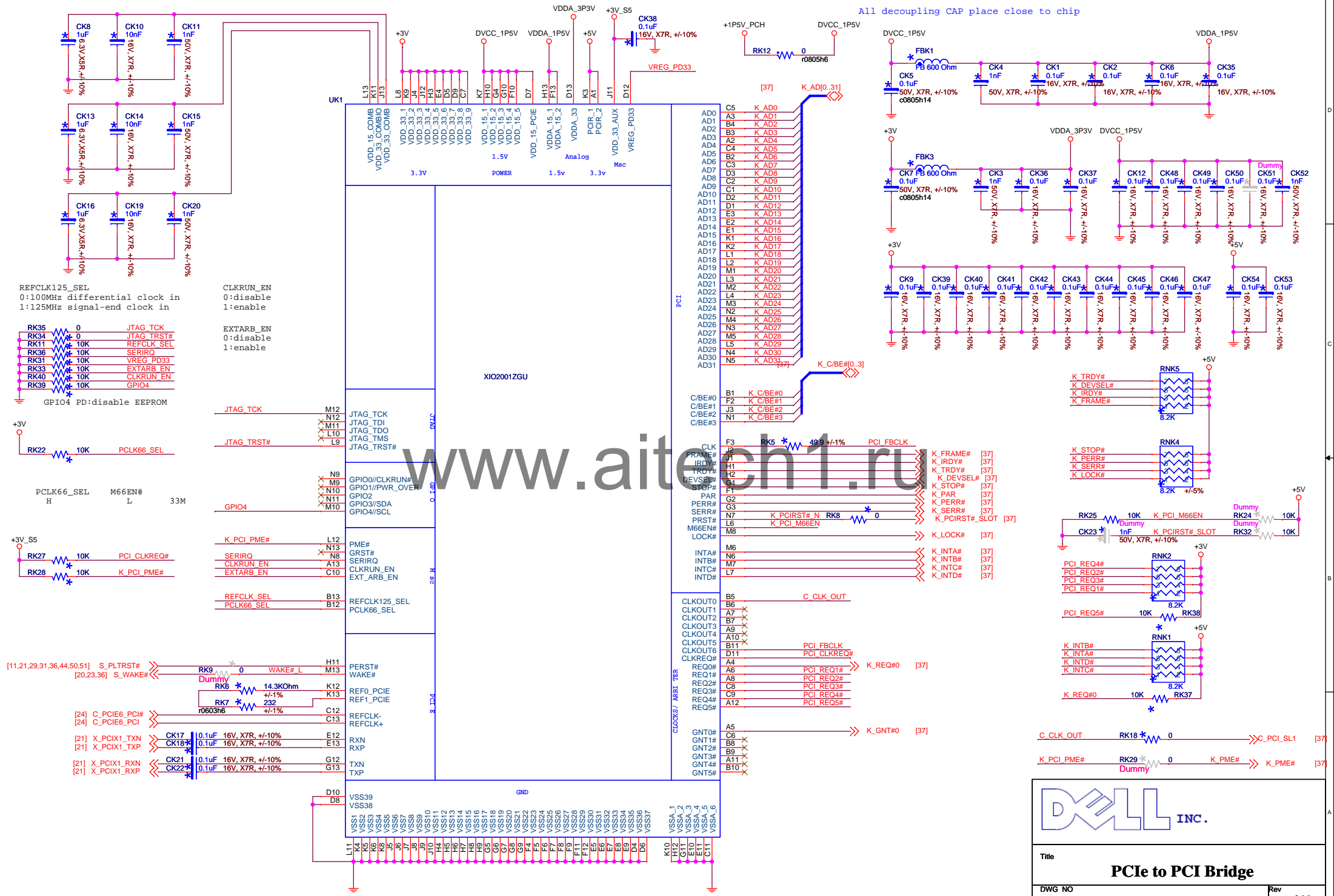


Figure 2-1: USB3 ICC pin numbering





Title

PCIe to PCI Bridge

DWG NO

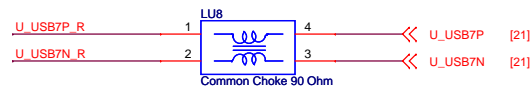
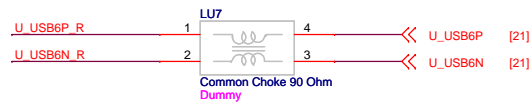
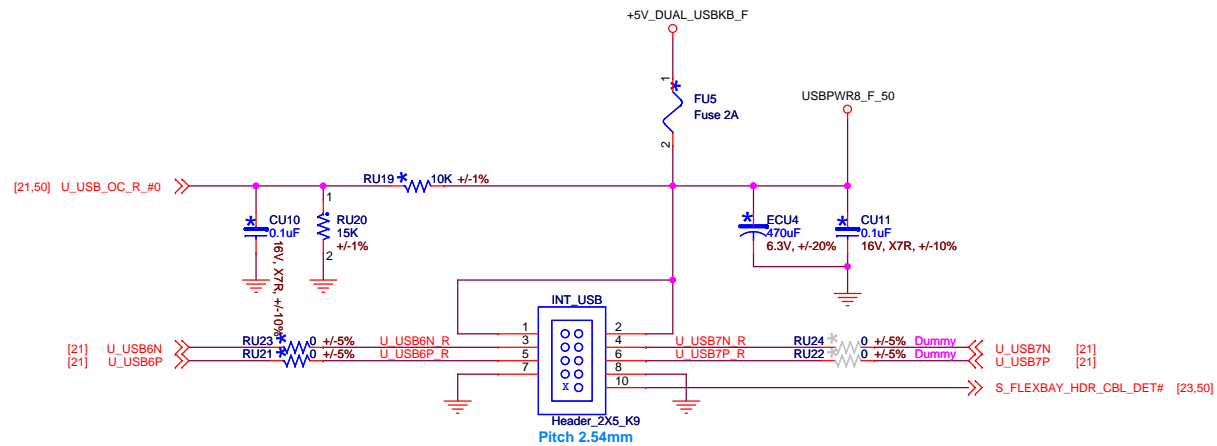
Tulum/Amazon MT

Date: Tuesday, January 29, 2013

Rev

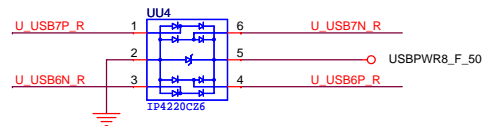
A00

Sheet 55 of 66

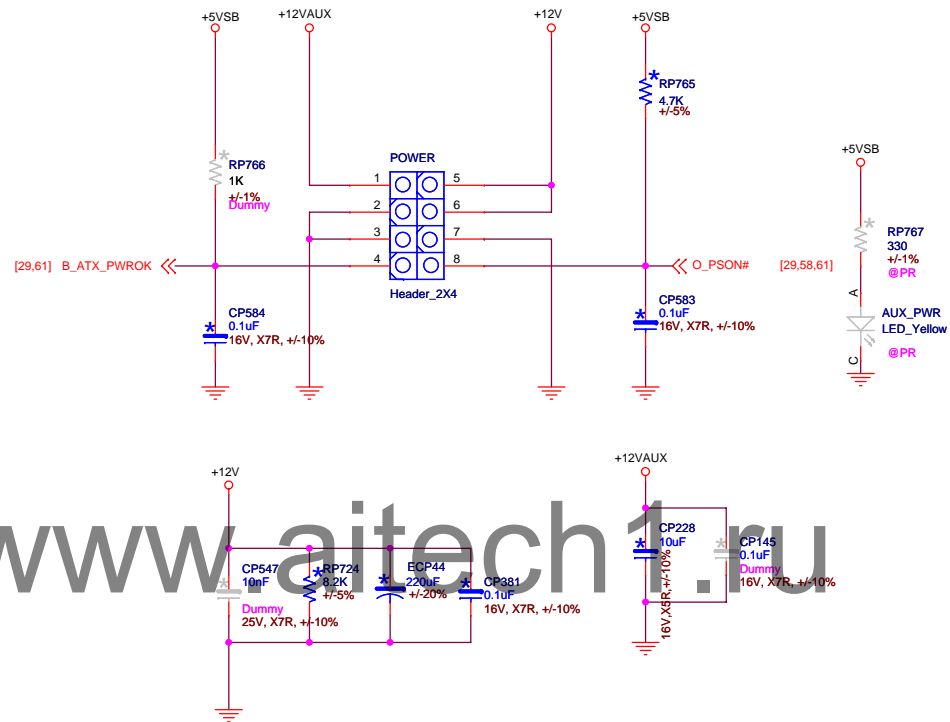


CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24

www.aitech1.ru

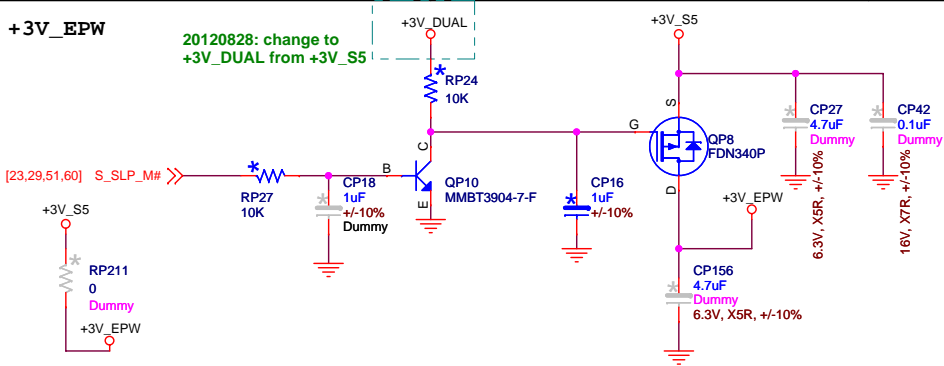


| | |
|---------------------------------|----------------|
| | |
| | |
| Title | |
| Internal USB | |
| DWG NO | Rev |
| Tulum/Amazon MT | A00 |
| Date: Tuesday, January 29, 2013 | Sheet 56 of 66 |



+3V_EPW

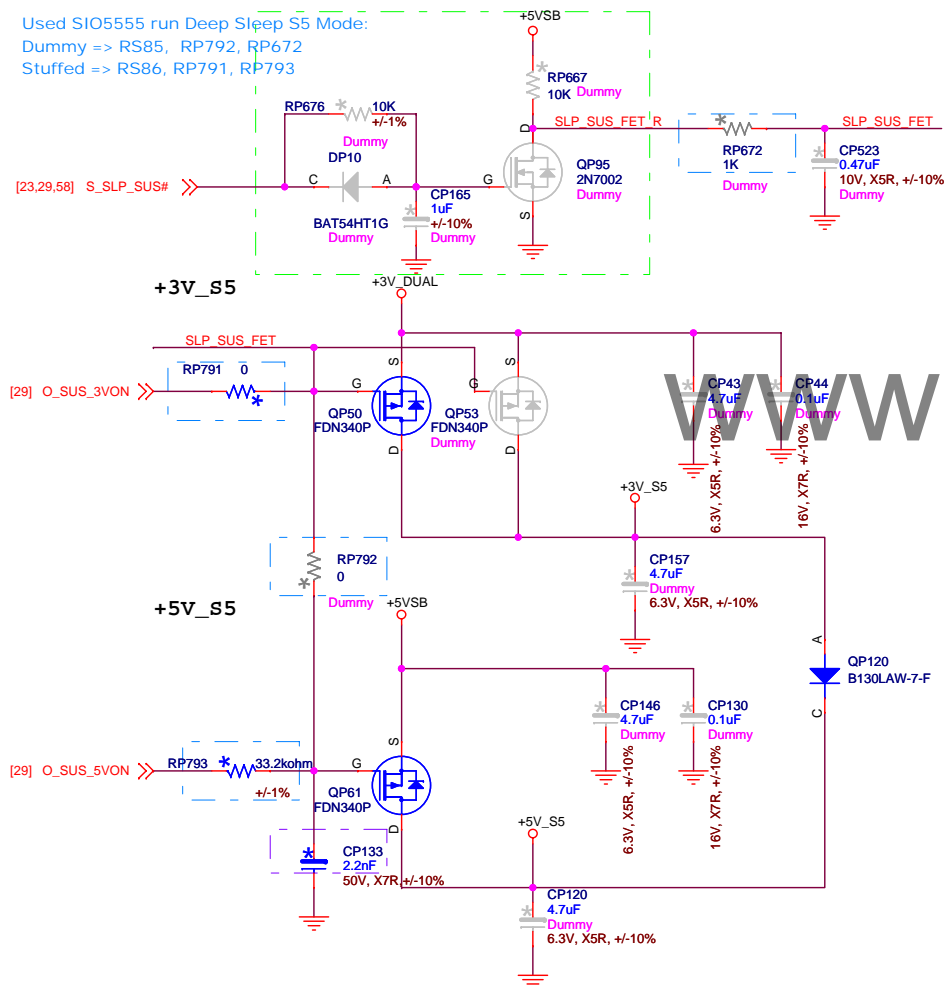
20120828: change to
+3V_DUAL from +3V_S5



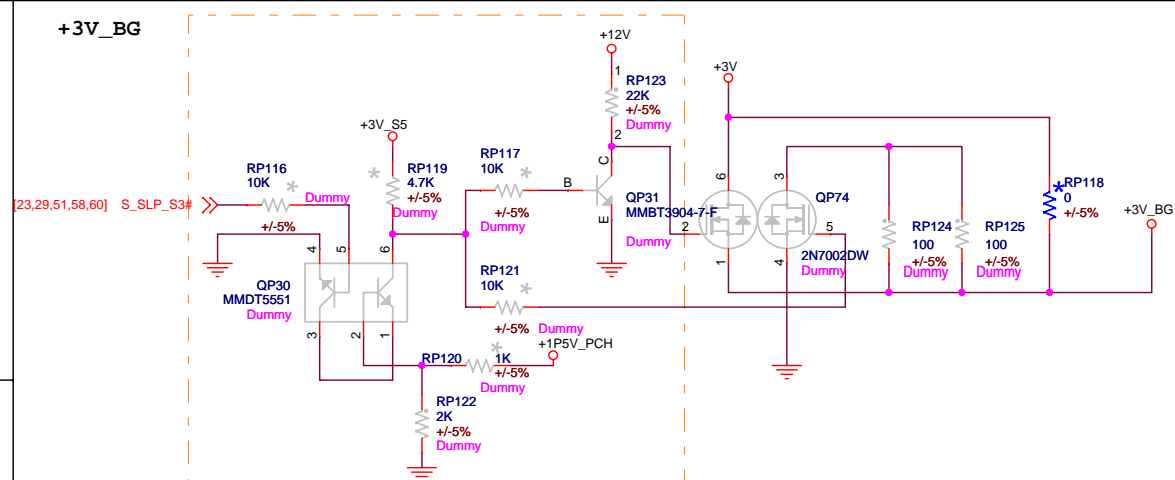
Used SIO5555 run Deep Sleep S5 Mode:

Dummy => RS85, RP792, RP672

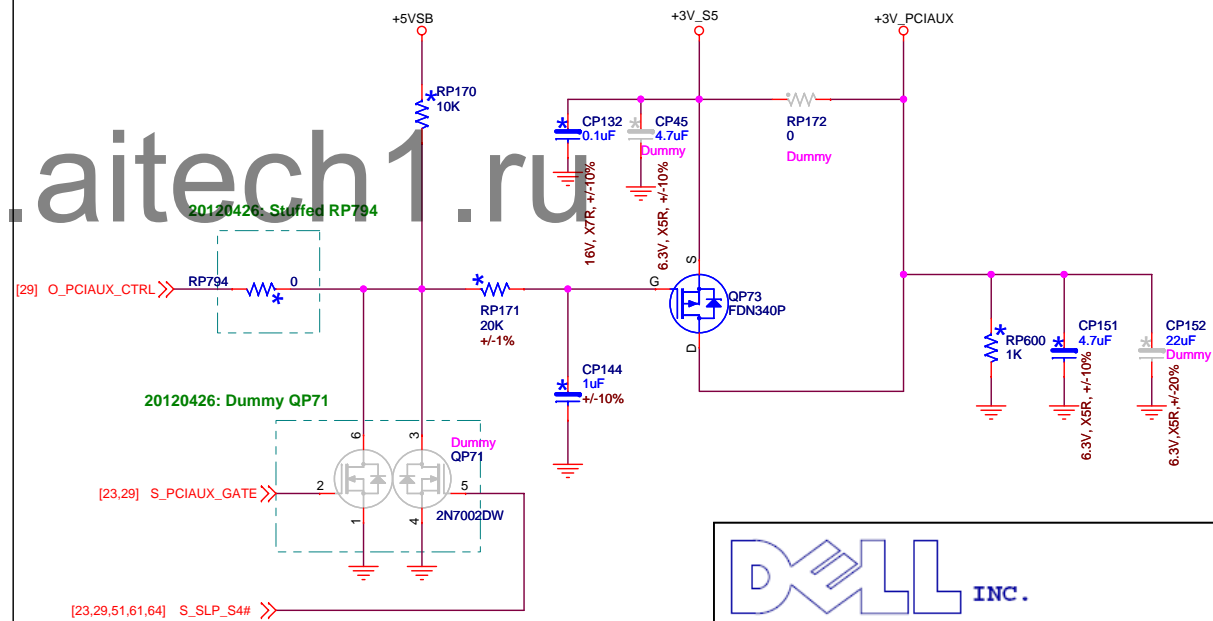
Stuffed => RS86, RP791, RP793



+3V_BG



+3V_PCIAUX(FOR PCI/PCIE SLOT)



Title

Power-1:Linear Power-1

DWG NO

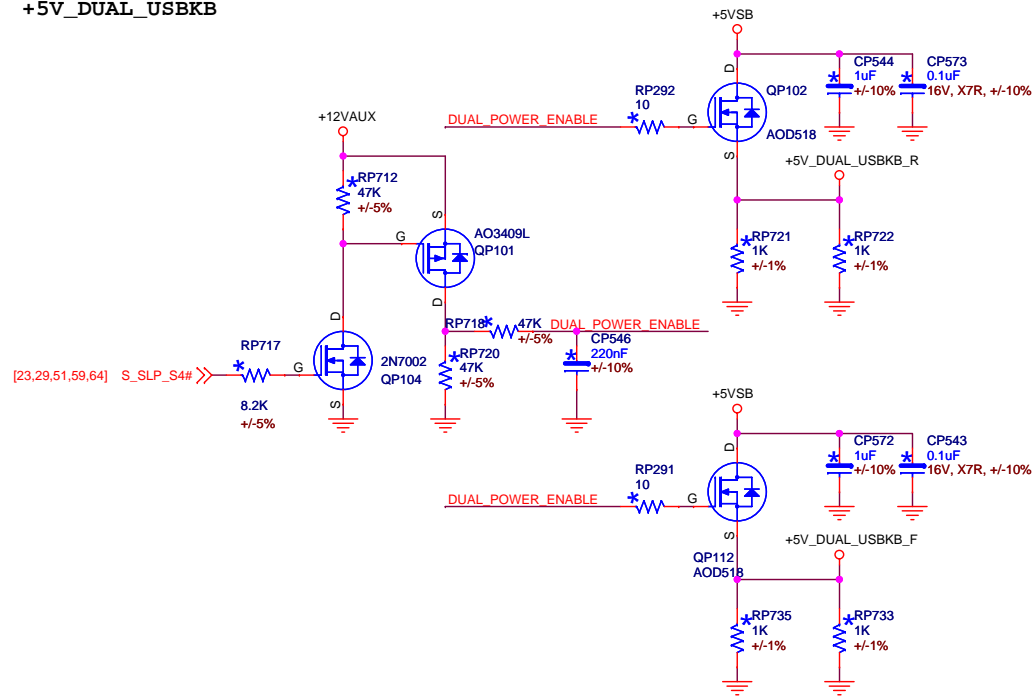
Tulum/Amazon MT

Rev
A00

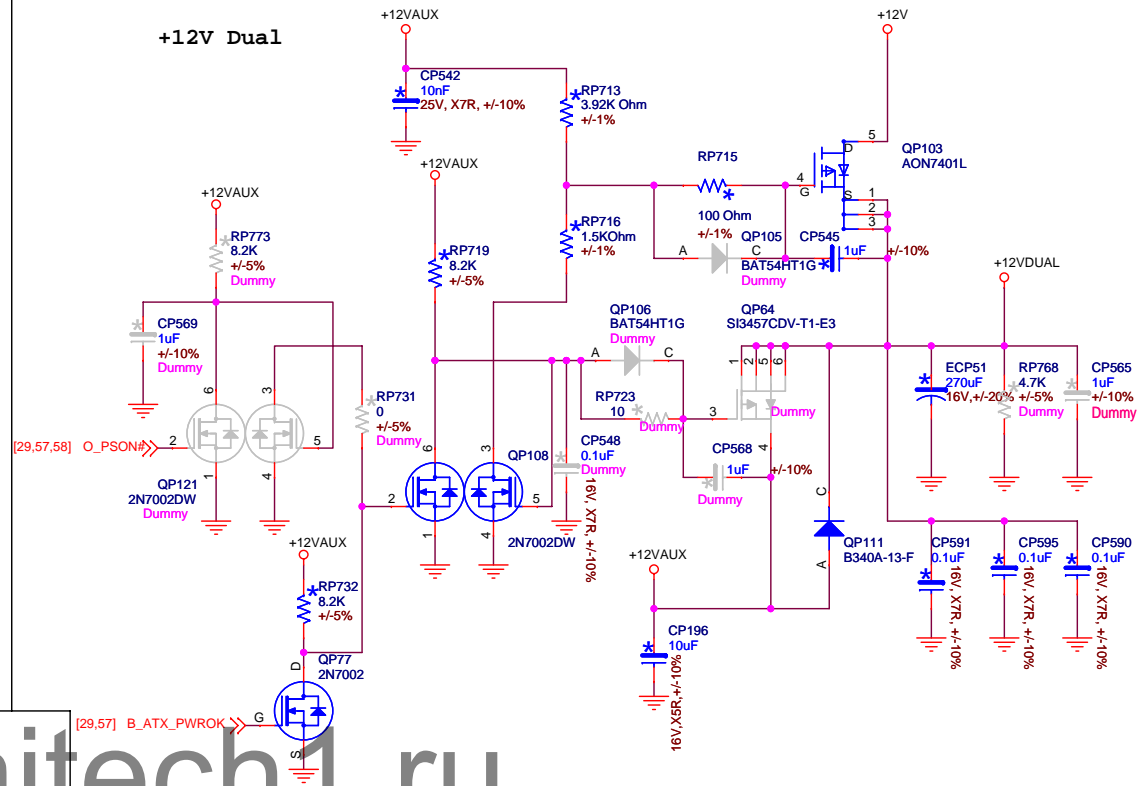
Date: Tuesday, January 29, 2013

Sheet 59 of 66

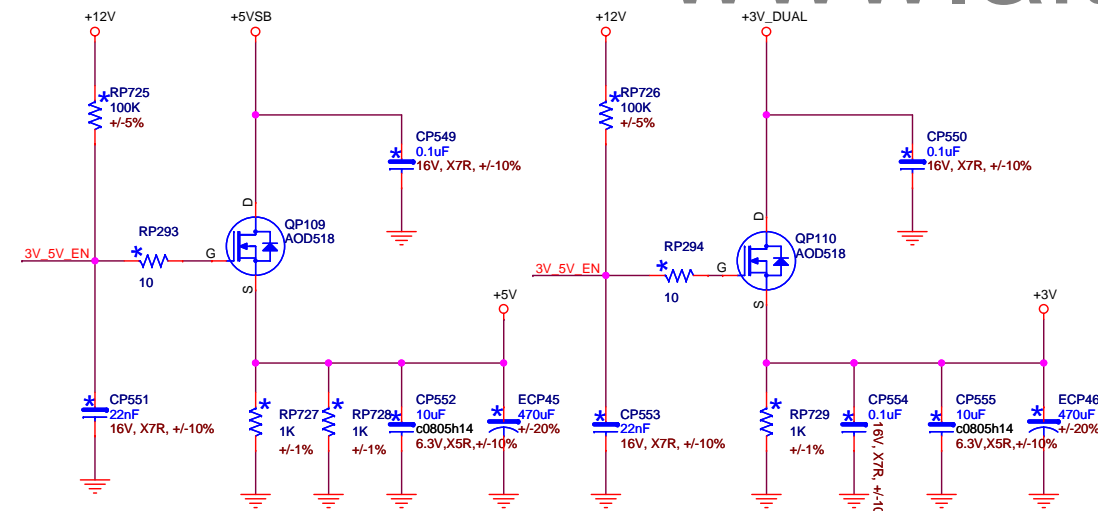
+5V_DUAL_USBKB



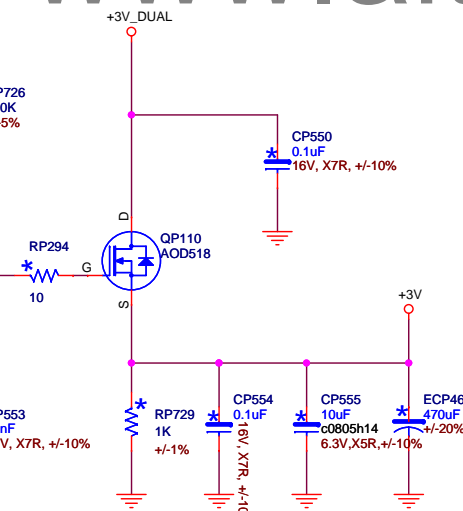
+12V Dual



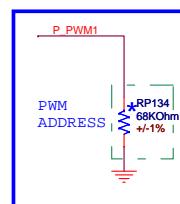
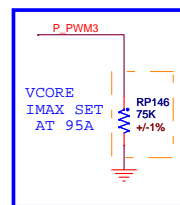
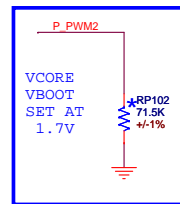
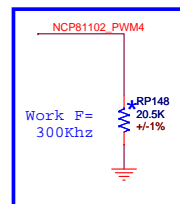
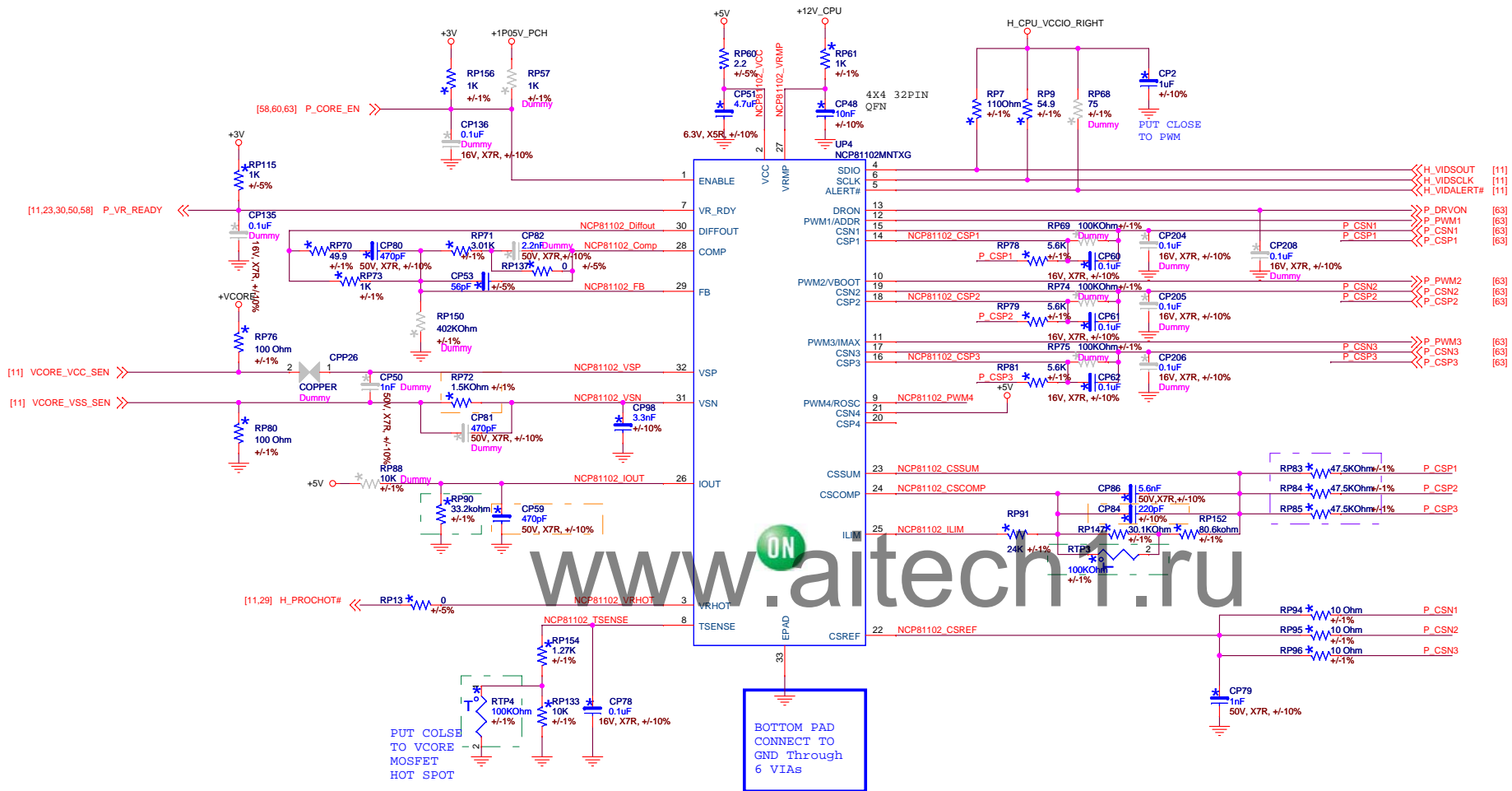
+5V MAIN



+3V MAIN



SharkBay VR12.5 POWER CKT -3PHASE

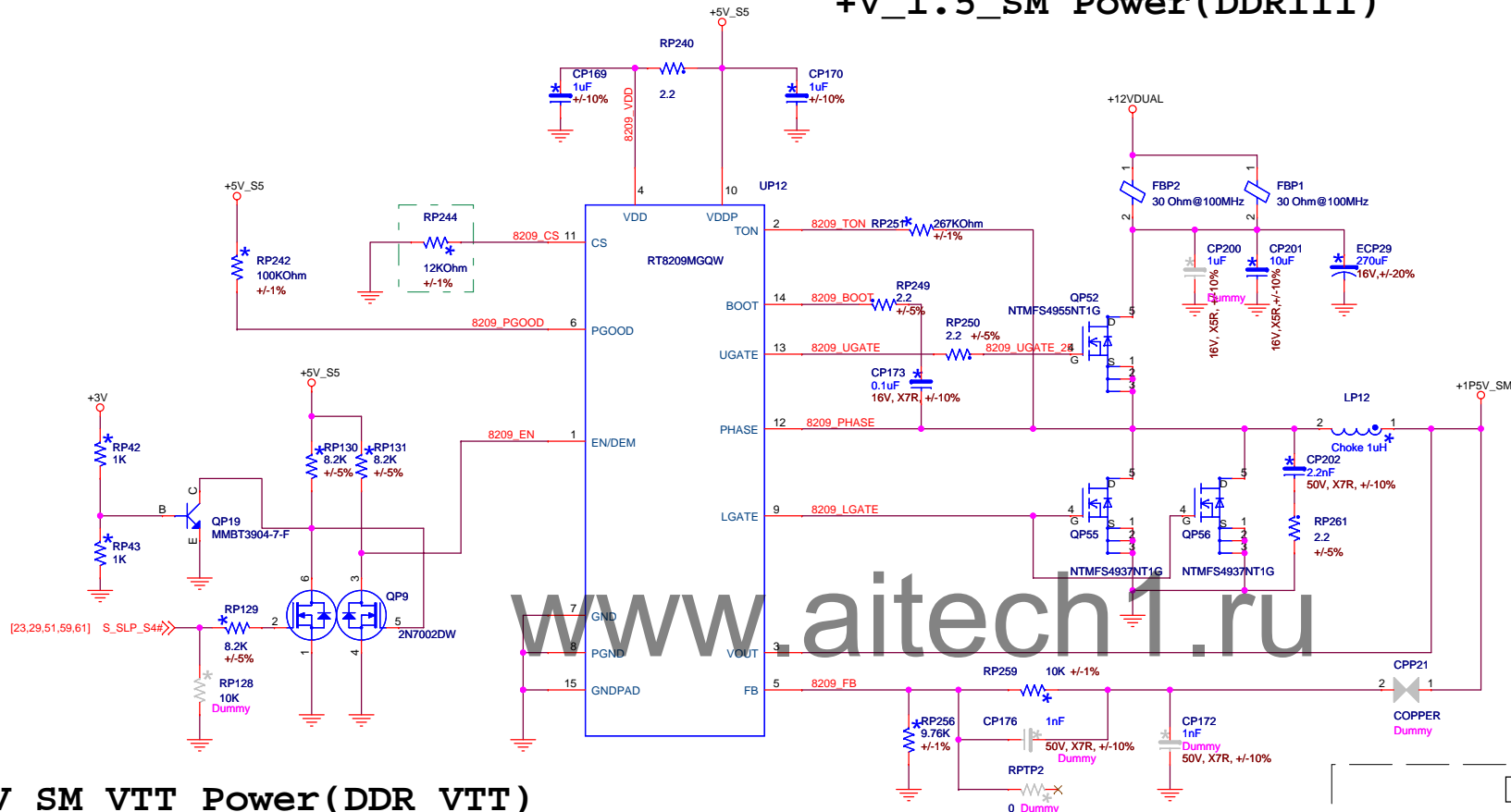


| Rosc | Freq. | Rosc | Freq. | Rosc | Freq. | Rosc | Freq. | Rosc | Freq. |
|-------|-------|-------|--------|-------|--------|-------|---------|------|--------|
| 10K | 250Kh | 30.9K | 340khz | 61.9K | 430Khz | 105K | 520 Khz | 165K | 610Khz |
| 12K | 260Kh | 34K | 350Khz | 64.9K | 440Khz | 110K | 530Khz | 174K | 620Khz |
| 14K | 270Kh | 36.5K | 360Khz | 69.8K | 450Khz | 115K | 540Khz | 182K | 630Khz |
| 16.2K | 280Kh | 40.2K | 370Khz | 73.2K | 460Khz | 121K | 550Khz | 191K | 640Khz |
| 18.2K | 290Kh | 43.2K | 380Khz | 78.7K | 470Khz | 130K | 560Khz | 200K | 650Khz |
| 20.5K | 300Kh | 46.4K | 390Khz | 82.5K | 480Khz | 137K | 570Khz | | |
| 23.2K | 310Kh | 49.9K | 400Khz | 88.7K | 490Khz | 143K | 580Khz | | |
| 25.5K | 320Kh | 53.6K | 410Khz | 93.1K | 500Khz | 150 K | 590Khz | | |
| 28K | 330Kh | 57.6K | 420Khz | 100K | 510Khz | 158 K | 600Khz | | |

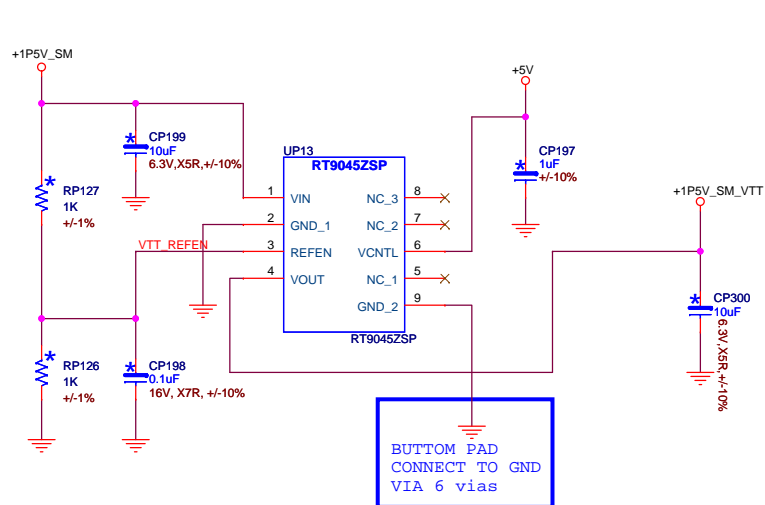


| | | | |
|----------------------|-------------------------------|-------------|----------------|
| Title | | | |
| Power-4:VCore | | | |
| DWG NO | <i>Tulum/Amazon MT</i> | | Rev A00 |
| Date: | Tuesday, January 29, 2013 | Sheet 62 of | 66 |

+V_1.5_SM Power(DDRIII)

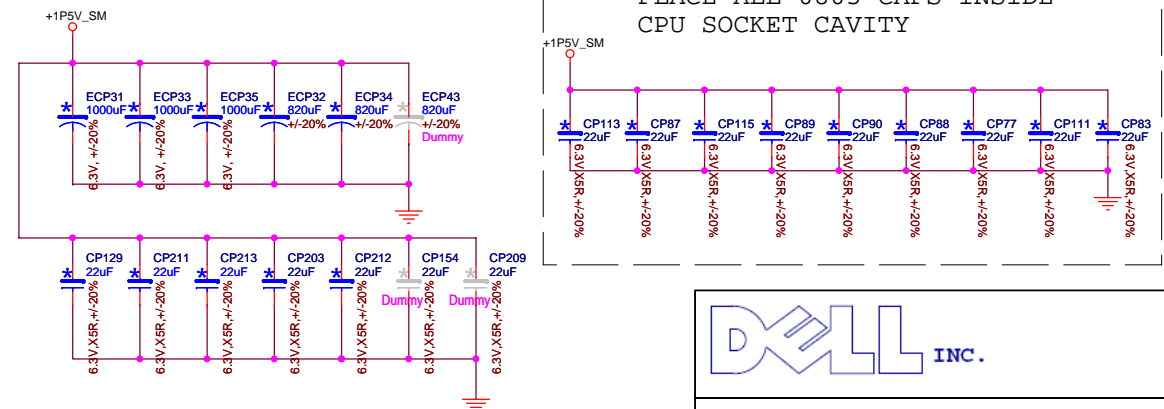


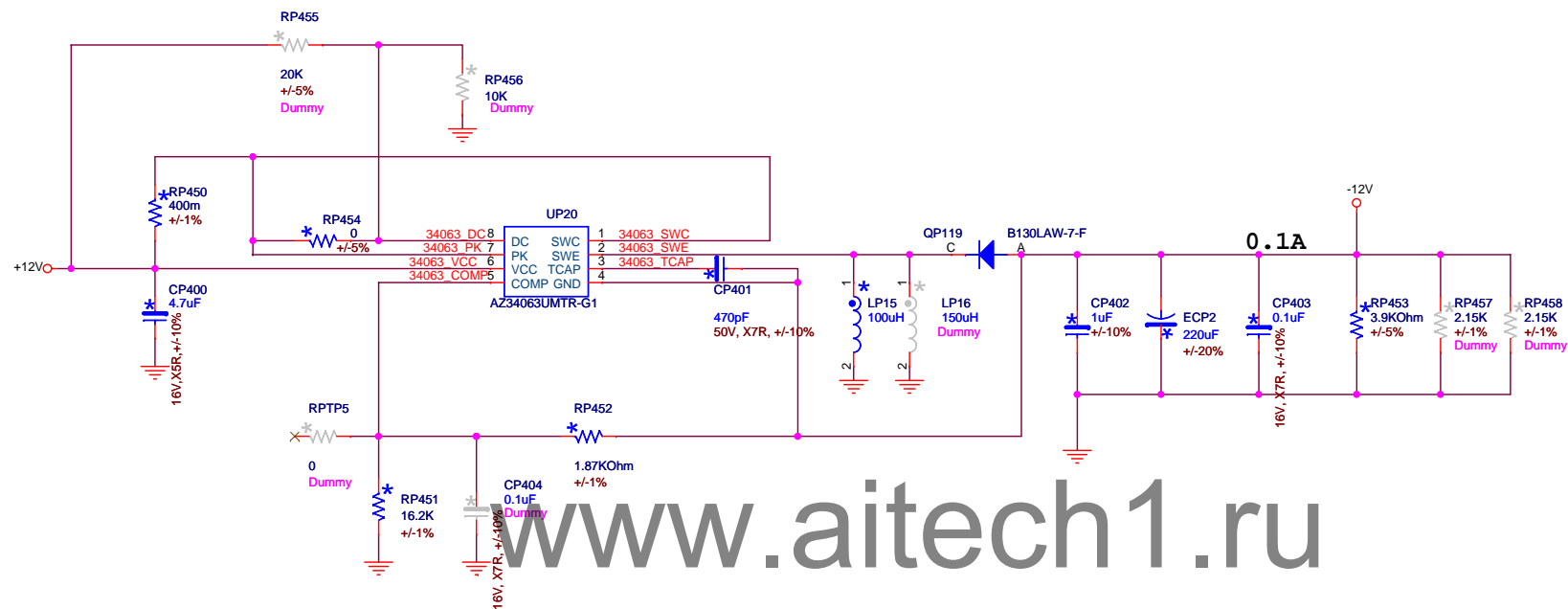
+V_SM_VTT Power(DDR VTT)




CAD NOTE:

PLACE ALL 0805 CAPS INSIDE
CPU SOCKET CAVITY





| | | |
|---|-----------------|---------|
|  | | |
| Title | | |
| Power-8: -12V | | |
| DWG NO | Tulum/Amazon MT | Rev A00 |
| Date: Tuesday, January 29, 2013 | Sheet 66 | of 66 |